Control of Pore Characteristics of Porous Silicon Using Non-toxic Electrochemical Etching for Photovoltaics and Supercapacitor Applications

Utpal Saha
South Dakota State University

Follow this and additional works at: http://openprairie.sdstate.edu/etd

Part of the Materials Science and Engineering Commons, and the Power and Energy Commons

Recommended Citation
http://openprairie.sdstate.edu/etd/1676

This Thesis - Open Access is brought to you for free and open access by Open PRAIRIE: Open Public Research Access Institutional Repository and Information Exchange. It has been accepted for inclusion in Theses and Dissertations by an authorized administrator of Open PRAIRIE: Open Public Research Access Institutional Repository and Information Exchange. For more information, please contact michael.biondo@sdstate.edu.
CONTROL OF PORE CHARACTERISTICS OF POROUS SILICON USING NON-TOXIC ELECTROCHEMICAL ETCHING FOR PHOTOVOLTAICS AND SUPERCAPACITOR APPLICATIONS

BY

UTPAL SAHA

A thesis submitted in partial fulfillment of the requirements for the Master of Science Major in Electrical Engineering South Dakota State University 2017
CONTROL OF PORE CHARACTERISTICS OF POROUS SILICON USING NON-TOXIC ELECTROCHEMICAL ETCHING FOR PHOTOVOLTAICS AND SUPERCAPACITOR APPLICATIONS

This thesis is approved as a credential and independent investigation by a candidate for the Master of Science degree and is acceptable for meeting the thesis requirement for this degree. Acceptance of this thesis does not imply that the conclusions reached by the candidate are necessarily the conclusions of the major department.

Quan Qiao, Ph.D.                                   Date
Thesis Adviser

Steven Hietpas, Ph.D.                              Date
Head, Department of Electrical
Engineering and Computer Science

Dean, Graduate School                            Date
ACKNOWLEDGEMENTS

I would like to express my sincere gratitude to my advisor Dr. Qiquan Qiao for giving me an opportunity to work in his group and serve as my thesis adviser at the Department of Electrical Engineering, Center for Advanced Photovoltaics, South Dakota State University. His continuous motivation, support, and criticism during research work until the completion of my thesis was tremendous and above all he had extreme faith on me. I am thankful to Dr. Prashu Kharel and Dr. Gary Hatfield for being in my thesis committee, and reviewing my thesis. I am also grateful to Dr. Fan for being my initial thesis supervisor.

I am very much indebted to Ezaldeen and Dr. Mahesh for their guidance and analysis process during the research work in numerous ways. I am thankful to Nezam Uddin, Khan Reza, Rajesh Pathak, Dr. Hytham Elbony, Ashim Gurung and many others for their invaluable support and suggestion for making this work possible.

I am grateful to my parents and my elder brother for their support and encouragement. Finally, thanks to all the graduate students of electrical engineering department for their wonderful company.
# TABLE OF CONTENTS

LIST OF FIGURES ........................................................................................................ vii

LIST OF TABLES ........................................................................................................... xi

ABSTRACT .................................................................................................................... xii

Chapter 1 Introduction ................................................................................................. 1
  1.1 Background ............................................................................................................. 1
  1.2 Previous work ....................................................................................................... 7
  1.3 Motivations .......................................................................................................... 10
  1.4 Objectives ............................................................................................................ 10

Chapter 2 Theory ........................................................................................................ 11
  2.1 Material Classification: Semiconductor ............................................................... 11
  2.2 Energy Band Origination ..................................................................................... 14
  2.3 Semiconductor Classification Based on Bandgap ................................................. 16
  2.4 Methods for Porous Silicon Fabrication ............................................................. 17
  2.5 Porous Silicon Formation .................................................................................... 18
  2.6 Surface Topography of Formed Pores ................................................................. 21
  2.7 Porous Silicon in PV Application ......................................................................... 22
  2.8 Porous Silicon as a Supercapacitor ..................................................................... 24
  2.9 Photoluminescence Spectroscopy of Porous Silicon ........................................... 26
  2.10 Raman Spectroscopy of Porous Silicon ............................................................... 27
2.11 Scanning Electron Microscope (SEM) .......................................................... 28

2.12 Electrochemical Characterization ................................................................ 29
    2.12.1 Electrochemical Impedance Spectroscopy (EIS) ............................... 29
    2.12.2 Cyclic Voltammetry (CV) Analysis .................................................. 31

Chapter 3 Experimental Procedure .................................................................. 34
    3.1 Fabrication of Porous Silicon ................................................................. 34
        3.1.1 Substrate Cleaning ........................................................................ 34
        3.1.2 Electrochemical Anodization ......................................................... 35
        3.1.3 Gold Deposition on Porous Silicon ................................................. 37
        3.1.4 Supercapacitor Fabrication ............................................................. 38
    3.2 Scanning Electron Microscope ................................................................. 39
    3.3 Optical Characterization ......................................................................... 40
        3.3.1 Reflectance .................................................................................... 40
        3.3.2 Raman Spectroscopy ..................................................................... 42
        3.3.3 Photoluminescence Spectroscopy ................................................... 43
    3.4 Electrochemical Measurements ............................................................... 44
        3.4.1 Electrochemical Impedance Spectroscopy ....................................... 44
        3.4.2 Cyclic Voltammetry Measurement ................................................. 45

Chapter 4 Results and Analysis ..................................................................... 46
    4.1 Characterization of Surface topography ................................................ 46
4.1.1 SEM Images of Porous Silicon ................................................................. 46
4.1.2 Calculation of Poroisty ............................................................................ 50
4.2 Optical Characterization of Porous Silicon ............................................ 53
  4.2.1 Reflectance Measurement of Porous Silicon ........................................ 53
  4.2.2 Photoluminescence Properties of Porous Silicon Samples ................. 59
  4.2.3 Raman Analysis of Porous silicon ......................................................... 62
4.3 Supercapacitor Characteristics of Porous Silicon ................................. 65
  4.3.1 Electrochemical Impedance Spectroscopy (EIS) Analysis .................. 65
  4.3.2 Cyclic Voltammetry (CV) Analysis of Porous Silicon ....................... 69
4.4 SEM Analysis of Passivated Porous Silicon Samples ......................... 71
4.5 Supercapacitor Characteristics of Passivated Samples ....................... 73

Chapter 5: Summary and Conclusions .......................................................... 79
  5.1 Summary ................................................................................................. 79
  5.2 Conclusions ............................................................................................ 81
  5.3 Future Tasks ............................................................................................ 82

References ....................................................................................................... 83
LIST OF FIGURES

Figure 1.1 Percentile comparison of green-house gas emission by various energy sources [3]........................................................................................................................................................................... 2

Figure 1.2 Electricity produced by different power plants [4]........................................................................... 2

Figure 2.1 Energy band diagram for an intrinsic semiconductor [36].................................................. 12

Figure 2.2 Electronic structure of (a) n-type Si and (b) p-type Si [37].............................................. 13

Figure 2.3 Energy band diagram of (a) n-type and (b) p-type semiconductor [38].............. 14

Figure 2.4 Schematic diagram illustrating the energy-band formation [39]............................. 15

Figure 2.5 Illustration of (a) direct and (b) indirect bandgap semiconductor by E-K diagram [41].......................................................................................................................................................... 17

Figure 2.6 Process-wise illustration of silicon anodization and dissolution [18]............. 20

Figure 2.7 (a) Illustration of the antireflection coating and (b) cross-section view of the structure of porous silicon [59] [60]......................................................................................... 23

Figure 2.8 Charging and discharging principle of a supercapacitor [63] ................. 25

Figure 2.9 Schematic diagram of a supercapacitor incorporating (a) EDL effect and (b) pseudo-capacitance effect [64, 65] .................................................................................................................. 26

Figure 2.10 Various types of Raman scattering during the Raman spectroscopy [74].... 27

Figure 2.11 Operational block diagram of a scanning electron microscope [80].............. 29

Figure 2.12 (a) the standard EIS plot and (b) the equivalent circuit of a supercapacitor [82].................................................................................................................................................................................. 31

Figure 2.13 Input voltage waveform applied in Cyclic Voltammetry measurement [84] 33

Figure 2.14 Standard output plot from CV showing the peak cathodic and anodic current [85]........................................................................................................................................................................... 33
Figure 3.1 Photographs of (a) the Sample holder and (b) the Ultrasonic cleaner used during cleaning of Si sample ................................................................. 35

Figure 3.2 Experimental set-up of electrochemical anodization process ................. 36

Figure 3.3 Photograph of the CRC-150 Sputtering system used for gold-deposition ...... 38

Figure 3.4 Photograph of the SEM used for the surface topography analysis ............ 40

Figure 3.5 Experimental set-up of the reflectance measurement using Filmetrics software .................................................................................................................. 42

Figure 3.6 Photograph of the Raman spectrometer set-up for Raman spectroscopy measurement ........................................................................................................... 43

Figure 3.7 Photograph of the Edinburgh Xe-900 photoluminescence spectrometer ...... 44

Figure 4.1 SEM image of porous silicon formed by Potentiostatic anodization (20 minutes) using anodization voltage of (a) 45V and (b) 50V ................................. 47

Figure 4.2 SEM image of porous silicon formed by galvanostatic anodization (20 minutes) using anodization current density of (a) 10 mA/cm² and (b) 20 mA/cm² ....... 48

Figure 4.3 SEM image of porous silicon formed by Potentiostatic anodization (90 volts) using anodization time of (a) 10 minutes and (b) 30 minutes................................. 49

Figure 4.4 Effect of variation of (a) voltage on porosity (b) current on porosity and (c) time on porosity ........................................................................................................... 52

Figure 4.5 Reflectance comparison of porous silicon samples fabricated by different values of anodization voltages ................................................................................. 54

Figure 4.6 Reflectance comparison of the porous silicon samples fabricated by CC method .................................................................................................................. 56
Figure 4.7 Reflectance spectra for porous silicon sample fabricated for 10 minutes of anodization for three different regions (region-1, region-2 and region-3) .................. 57

Figure 4.8 Reflectance spectra for porous silicon sample fabricated for 30 minutes of anodization for three different regions (region-1, region-2 and region-3) ............... 58

Figure 4.9 Average Reflectance comparison among (a) voltage (b) current density and (c) time ........................................................................................................................................ 59

Figure 4.10 Photoluminescence spectra of porous silicon samples formed by CV method of anodization ................................................................................................................. 61

Figure 4.11 Photoluminescence spectra of porous silicon samples formed by CC method of anodization ................................................................................................................. 61

Figure 4.12 Surface topography obtained during Raman spectroscopy for porous silicon samples prepared using anodization voltage of (a) 45V and (b) 50V ......................... 62

Figure 4.13 Raman spectra of porous silicon samples fabricated by different values of voltage ........................................................................................................................................ 63

Figure 4.14 Surface topography obtained during Raman spectroscopy for porous silicon samples using current density of (a) 30mA/cm$^2$ and (b) 40mA/cm$^2$ ....................... 64

Figure 4.15 Raman spectra of porous silicon samples fabricated by different values of current density ................................................................................................................. 65

Figure 4.16 EIS spectroscopy showing the Nyquist plot of the PS sample fabricated by the CV (45V) method ................................................................................................................. 67

Figure 4.17 EIS spectroscopy showing the Nyquist plot of the PS sample fabricated by the CC (10mA) method ................................................................................................................. 68
Figure 4.18 CV measurement of supercapacitor cells fabricated using PS cells prepared by potentiostatic (45V) method .......................................................... 70

Figure 4.19 CV measurement of supercapacitor cells fabricated using PS cells prepared by Galvanostatic (10mA/cm²) method............................................................. 71

Figure 4.20 SEM image of porous silicon sample (10mA/cm²) after passivated by gold sputtering............................................................................................................. 72

Figure 4.21 Nyquist plot of the supercapacitor device fabricated by using passivated porous silicon samples (10mA/cm²)................................................................. 74

Figure 4.22 CV plot of the supercapacitor device fabricated by using passivated porous silicon samples (10mA/cm²)........................................................................... 75

Figure 4.23 Nyquist plot of the supercapacitor device fabricated by using passivated porous silicon samples (45V)................................................................. 76

Figure 4.24 CV plot of the supercapacitor device fabricated by using passivated porous silicon samples (45V) ................................................................. 77
LIST OF TABLES

Table 4. 1 Porosity for different etching parameters ......................................................... 51
Table 4. 2 Parameters calculated from EIC spectroscopy for the porous silicon .......... 68
Table 4. 3 Parameters calculated from EIC spectroscopy for the passivated porous silicon supercapacitors ............................................................................................................. 78
ABSTRACT

CONTROL OF PORE CHARACTERISTICS OF POROUS SILICON USING NON-TOXIC ELECTROCHEMICAL ETCHING FOR PHOTOVOLTAICS AND SUPERCAPACITOR APPLICATIONS

UTPAL SAHA

2017

Porous silicon has exhibited lower reflectance and higher surface area than the pristine silicon. This property of porous silicon can be applied to photovoltaic (PV) application for more efficient silicon solar cells and for higher performance of supercapacitors. \( \text{NH}_4\text{Fl} \) electrolytic etching solution has been used to fabricate porous silicon, but the control of pore morphology of silicon is achieved only by controlling the time. Therefore, it is urgently required to use other etching parameters such as voltage and current to achieve flexible control of pore properties. Porous silicon can also be used to fabricate supercapacitors. An established approach to make it applicable for higher performance supercapacitors is to passivate of the surface and modify its surface properties.

In this report, porous silicon has been fabricated by electrochemical anodization method using a non-toxic ammonium-fluoride (\( \text{NH}_4\text{Fl} \)) based electrolytic solution. Control of pore characteristic has been achieved by flexible control of etching parameters such as voltage, current and time. Higher performance supercapacitors have been made by passivating the porous silicon surface with a thin layer of gold deposition.
Chapter 1 Introduction

1.1 Background

As the world population is increasing day by day, the energy demand is also increasing proportionally. The rapid growth of industries and increasing use of energy especially by the developed nations has also played a vital role in the increase of the demand for energy. Nuclear energy and fossil fuels are the two most common sources of energy. Each of these sources have their own disadvantages. Non-renewable fossil fuels produce carbon-dioxide when it is burnt. carbon-dioxide is responsible for the greenhouse effect [1] and the gradual reduction of the ozone layer.

Acid rain is the ultimate by-product of burning fossil fuels. When fossil fuel is burnt, sulfur oxides (SiO\textsubscript{x}) and nitrogen oxides (NO\textsubscript{x}) are produced. These oxides react with water and oxygen to produce acid rain. As far as USA is concerned, about 25% of NO\textsubscript{x} and 67% of SiO\textsubscript{x} are produced by electrical power plants [2]. These power plants mainly use fossil fuels for their production of electrical energy. The following comparison shown in figure 1.1 and figure 1.2 will present a clear view about sources of energy and their corresponding production of the harmful greenhouse gases.
Figure 1.1 Percentile comparison of green-house gas emission by various energy sources [3]

Figure 1.2 Electricity produced by different power plants [4]
The nuclear power plants contribute about 11% of the total produced electricity. The operating principle of these plants is very harmful to the environment. In these types of plants, heavy metals and salts react with water [5]. The water gets contaminated during this process. Therefore, when this water is disposed of in the environment, it causes a great water pollution. Another dangerous effect of nuclear power plants is the radioactive effect which is caused by the Uranium fuel used to produce electricity. To dispose of the burnt Uranium, these plants are shut down for several days (15-20 days) [6]. When the burnt Uranium is disposed of in the environment, it causes severe health hazard due to the radioactive interference that the Uranium contains. There are numerous reports which show that how dangerous the nuclear power plants can be for all living beings on earth. Therefore, it is very important to look for alternative sources of energy and solar energy can be one of the most effective sources.

As the countries are getting more and more developed in terms of improved lifestyle and quality, the demand for electrochemical energy storage has increased rapidly. Batteries and supercapacitors are two main devices that explore the electrochemical energy storage. There is a growing need to produce more efficient and lower cost devices using cheaper materials. Although existing techniques for fabricating supercapacitors tend to produce a significant amount of electrochemical energy, most of them use materials that are very expensive. Their fabrication techniques are somewhat complicated too. Most of the supercapacitors are made by carbon and nickel [7]. The main drawbacks associated with this type of fabrication are complicated production technique and expensive experimental set-up. Therefore, it is also extremely important to fabricate cost effective supercapacitors that use cheaper materials and simple production procedures.
Solar cells generate electrical power using solar energy that comes from the sun. The availability of the input solar energy is very high. Solar cells are gradually replacing the conventional power plants to produce electricity. It is entirely clean as there is no emission during the process of conversion from sunlight to electricity. Solar energy can be defined as the combination of heat and light that is radiated from the sun [8]. It is available in enormous amount in nature. Annual energy produced by the sun can be as high as 1575-49,837 exajoules (EJ) [8]. This is much higher than the global energy consumption in 2012 which was around 559.8EJ [8]. Therefore, solar cells have an amazing prospect to meet the global energy demand. Most the solar cell industries are dependent on silicon-based solar cells. Silicon is a semiconductor that is extensively used in other industries such as Very Large Scale Integration (VLSI) industry to make transistors. In VLSI industries, a huge number of transistors are integrated in a single chip. The very first silicon solar cell in the history was reported by R. S. Ohl in 1941[9]. It had only 1% efficiency. Since then, numerous researchers have been trying to increase the efficiency. As far as Si solar cells are concerned, highest reported efficiency to date is around 25% as reported by UNSW PERL [10].

Sunlight is converted into electrical power by some specified steps. At first, the sunlight is absorbed by the solar cell and then electron-hole pairs are generated. Secondly, these pairs are separated into charges of opposite signs and finally these charges are collected by the external load. When the sunlight falls upon the solar cell surface, the absorbance will be maximum if the reflectance and transmittance losses are minimum. An untreated silicon surface has a very high amount of reflectance which can be as high as 40%. Therefore, it can be understood that the efficiency of solar cells will
be highly improved if the reflection loss can be reduced as much as possible. To reduce reflectance, the untreated surface must be modified to an anti-reflective surface. One of the ways to reduce reflectance is to create an antireflection coating on the silicon surface. Anti-reflection coatings (ARC) can increase the efficiency of solar cells by more than 30%.

To generate ARC, several techniques and materials are used. Materials that have been generally used for antireflection coating (ARC) are SiO$_2$, TiO$_2$, Ta$_2$O$_5$, ZnS and CeO$_2$. These AR coatings are deposited by Chemical Vapor Deposition (CVD), splash, screen printing [11] and vanishing or sputtering. All of these techniques are complicated and expensive [12]. Lowest reflectance (10%) achieved by ARC in Si solar cells is usually made of silicon nitride [13, 14]. Multilayered structure of MgF$_2$/Al$_2$O$_3$/ZnS has been used to generate ARC that results in a reflectance under 3%. In these ARC structures, each layer is coated separately [15]. The fundamental disadvantage related with these ordinarily utilized materials is the necessity of numerous deposition, which eventually increases the overall cost. Likewise, PECVD (Plasma Enhanced Chemical Vapor Deposition) utilizes silane for silicon nitride antireflection coatings (ARC) and found in about all sunlight based cell fabricating organization. Therefore, the overall cost of capital investment and running procedure can be reduced by not using silane to produce ARC. In this regard, porous silicon has been utilized as antireflection layer for the proficient light trapping in photovoltaic solar cells.

Supercapacitors are the most effective devices to store electrochemical energy compared to conventional batteries and capacitors. Usually the stored capacity of supercapacitors is 10-100 times greater than the electrolytic capacitors. Charge-delivery
rate of supercapacitors are much faster compared to batteries and they can withstand a
greater number of charge-discharge cycles in comparison to rechargeable batteries [16].
Most of the available techniques use carbon and nickel electrodes to fabricate
supercapacitors. They use expensive fabrication method and lengthy production
procedure. Silicon is the second most abundant material on earth. Therefore, it would be
extremely effective to use silicon to make electrochemical supercapacitors. This can be
achieved by the surface modification of porous silicon samples.

Any silicon crystal that contains a series of holes or voids in the surface is a
porous silicon structure. Porous structure of silicon typically contains a thickness of
several microns that enables it to have a higher ratio of surface to volume compared to
the bare silicon surface. It is mostly used in Photovoltaic application (as an anti-reflection
coating), biomedical (biomaterials, in-vivo applications) sensing and very recently in
electrochemical energy storage application (supercapacitors).

Porous silicon (PS) offers cost effective and easy fabrication procedure.
Therefore, it can be extremely effective in Photovoltaic (PV) silicon solar cells and
electrochemical energy storage as a supercapacitor. Applications in PV industry is mainly
executed by the low reflectance characteristics of the porous structure. High surface area
enables it to be utilized in electrochemical energy storage applications. Reflectance
property can be effectively controlled by the variation of etching parameters.
Supercapacitors characteristics can be improved by the modification of porous silicon
surface.
1.2 Previous work

The discovery of porous silicon happened by an accident. In 1956, Arthur Uhlir Jr. and Ingeborg Uhlir were working on a project to modify the surface of silicon and germanium [17]. They were using HF based electrolyte and found out that the surface contained a coating of red-green film [17, 18]. The outcome fell way below expectations and the incident was only recorded for further reference.

In 1982, A. Prasad et al. [12] proposed the porous silicon for solar sell applications created by utilizing HF under light without outside biasing. However, the authors did not say about the morphology of porous silicon. No data was given about the control of pore properties and its effect in solar cell efficiency.

In 1986, Beale et al. [19] investigated stain scratching of silicon in HF, NaNO₂ or HF, CrO₃ to produce the porous layer. The thickness of porous silicon layer was restricted to a couple of microns which was the main disadvantage of the work.

In 1990, Leigh Canham [20] reported about photoluminescence from p-type silicon wafer produced electrochemically in HF based electrolytic solution. Although photoluminescence property showed by porous silicon opened new ways for optoelectronics application, there was no investigation about the control of pore morphology.

The assurance of reproducibility and flexible pore morphology was the major problem in the report of Vasquez et al. in 1990 [21] regarding the synthetic etching of silicon in a mixture of HF, HNO₃ and H₂O electrolytic solution.
After two years in 1992, Hummel et al. [22] showed a new method for porous silicon layer arrangement. Silicon wafer started to disintegrate when high voltage/low tesla transformer was used. This technique did not ensure about the repeatability of the porous structure; pore morphology was not uniform and porosity was not calculated.

There was an interesting investigation to fabricate porous coating with the help of magnetic fields published by Nakagawa et al. in 1996 [23]. However, there was no report of the porosity as well as the pore uniformity and the expansion of porosity with the magnetic field was 10% only.

The electrochemical etching of HF electrolytic solution was utilized to modify the surface of silicon as an anti-reflector for solar cells and was reported in 1998 by J. Zettner et al. [24]. The main limitation was that there was no investigation about controlling the reflectance property.

In 1999, S. E. Rowlands et al. reported about supercapacitors using electrodes of gold-coated porous silicon [25]. But it suffered from an extremely low value of capacitance (0.13mF/cm²) and the knee frequency was not used for the calculation of capacitance.

In early 2001, an article published by Splinter et al. [26] discussed a new process to produce porous silicon. He used HF electrolytic solution and external biasing for anodization. The experiment relied upon valuable metal and thickness of these metal layers. Valuable component (gold, platinum) was utilized to metallize the silicon. The report did not have essential data about pore morphology, thickness profile and
repeatability of the porous structure. The fabrication cost also increased because of using expensive elements.

Two years later in 2003, an ultrasonic-assisted electrochemical etching method to produce the porous silicon layer was proposed by Y. Liu et al. [27]. He used HF electrolytic solution which is toxic and can damage the surface properties of porous silicon.

Pulsed electrochemical anodization technique for the fabrication of p-type porous silicon was investigated in 2009 by Osorioa. E, et al. [28]. Electrochemical etching of silicon was performed utilizing 48% HF and 98% ethanol (1:1) based electrolyte and different values of current densities. The main disadvantage of this work was very slow diffusion of hydrogen air bubbles and silicon fluoride [27].

Then in 2010, J.H. Selj et al. [29] published an article about the fabrication of porous silicon as an anti-reflection coating and the porous silicon contained more than one layer of coating on the silicon surface. However, the publishers did not examine the consistency and morphology of the porous layers.

In 2010, xenon difluoride (XeF₂) dry drawing technique for the formation of porous silicon was reported by Hajj-Hassan M. et al. This procedure required a vacuum framework for the experimental set-up that makes it very expensive fabrication technique.

In 2011, Khaldun et al. [30] reported the effect of etching time on Porous silicon characteristics. But there was no investigation of the effect of voltage and current. He also used the toxic HF electrolytic solution.
In 2013, Manoj et al. [31] investigated the reflectance of PS samples by using NH$_4$Fl based electrochemical anodization technique. But the reflectance was reduced to only 10% and there was no survey of the photoluminescence and Raman spectroscopy. The major drawback was that they did not mention any application of his fabricated porous silicon samples.

In 2013, Fleur Thissandier et al. reported about ultra-capacitor with doped Si nanowires. But the overall capacitance was only 10μF/cm$^2$ [32].

In 2013, Landen Oakes et al. published a paper about electrochemical capacitors with graphene coating on Porous silicon surface [7]. But they used toxic HF solution to fabricate porous silicon which degrades the pore characteristics.

1.3 Motivations

Need to achieve lower reflectance of porous silicon for high-efficient Si solar cells and surface modification of porous silicon for better performance in supercapacitors.

1.4 Objectives

- Effectively control the porosity of porous silicon by the variation of electrochemical anodization parameters such as voltage, current and time to achieve low reflectance.
- Engineer reduction of oxidation of porous silicon by surface passivation to improve its performance in supercapacitors.
Chapter 2 Theory

2.1 Material Classification: Semiconductor

Based on electrical properties, all the materials are divided into three categories i.e. conductor, semiconductor and insulator. Semiconductors are very interesting as they have properties that lies between the conductor and the insulator. They have conductivity lower than that of the semiconductor but higher than the insulator.

The invention of certain semiconductors has redefined the human civilization and made amazing technological advancements. Silicon (Si), Germanium (Ge) and Tellurium (Te) [33] are the three most popular semiconductor materials. Most of the semiconductor research is focused on these semiconductors. Semiconductor itself can be subdivided into two groups such as intrinsic semiconductor and extrinsic semiconductor. Intrinsic semiconductor does not have any impurity in them which means that they are pure or undoped. This makes them enable to have equal amount of positive charges (holes) and negative charges (electrons). The electron and holes are created in a pair in intrinsic semiconductor by a method called thermal excitation. The relation between their concentrations \(n_i\) can be expressed by the following equation [34].

\[
n_i = N_s \exp\left(-\frac{E_g}{2k_B T}\right)
\]

Where, \(N_s\) = the number of effectively available states per unit volume;

\(E_g\) = the energy gap (between the bottom of the conduction band and the top of the valence band)

\(k_B\) = Boltzmann’s constant = \(1.381 \times 10^{-23}\) Joules/Kelvin and

\(T\) = the absolute temperature in Kelvin
The fermi level in an energy band is defined as the cumulative electric potential of the electrons [35]. The location of the fermi level indicates the type of material. As there is no impurity in an intrinsic semiconductor, there the fermi level lies exactly in the mid-gap of the energy band. The following figure 2.1 describes the energy band diagram of an intrinsic semiconductor with proper location of the various types of energy bands.

![Energy band diagram for an intrinsic semiconductor](image)

Figure 2.1 Energy band diagram for an intrinsic semiconductor [36]

On the other hand, extrinsic semiconductors are not pure and are subjected to doping. Based on the numeric value of the charge concentration, extrinsic semiconductor is subdivided into two different types. They are n-type semiconductor and p-type semiconductor. If the concentration of electron is greater than that of the holes, it is called n-type semiconductor. N-type semiconductors are generally created by doping the pure semiconductor with a material that contains five valence electrons in the outer shell.
Example of these types of materials in the periodic table are Arsenic (As), Phosphorous (P), Antimony (Sb) etc. These materials are usually called donor as they give away their electrons when added up with intrinsic semiconductor. The electronic structure of extrinsic semiconductors is shown in figure 2.2.

![Electronic structure of (a) n-type Si and (b) p-type Si](image)

**Figure 2.2** Electronic structure of (a) n-type Si and (b) p-type Si [37]

P-type semiconductors contain a higher concentration of holes than the electrons. P-type semiconductors are created by doping them with materials that have 3 valence electrons in their outer shell. These materials are termed as acceptor as they take out electrons from the materials and thereby create a vacancy in that material. These vacancies are called holes and therefore the concentration of holes are increased in the p-type semiconductor. Example of such materials in the periodic table that have 3 valence electrons in the outer shell are Boron (B), Aluminum (Al), Gallium (Ga), Indium etc. The band diagram of extrinsic semiconductors is shown in figure 2.3.
2.2 Energy Band Origination

There are mainly three types of energy bands in a crystal. The bands are called valence band, fermi level energy band and conduction band. Molecular orbitals are created by the combination of the atomic orbitals of two atoms when they are brought in close vicinity to each other. By this process, the equilibrium states of the energy bands are disturbed. This is consistent with Pauli’s exclusion principle [68]. Thus, band of energies are generated and they are continuous in nature. Without any external excitation, most of the electrons are in the lowest energy band known as valence band (VB). Highest energy band known as the conduction band (CB) contain very few electrons. The energy gap ($E_g$) is defined as the difference between the energy levels of VB and CB. This is also known as forbidden band due to the absence of any electrons in this band.
If a crystal consists of N atoms, the number of valence electrons will be 4N. The number of energy states in turn will be two times the number of valence electrons. Half of these must be empty while the other half can be occupied. The lowest energy level is occupied by the electrons when the temperature is 0K. Silicon has all the valence electrons located in the valence band at 0K. The conduction band discussed above remains free of charge carriers during this time. The basic orbital interaction by which the bands are formed is shown in figure 2.4.

The energy bands overlap in a solid metal and therefore it is very easy to excite the charge carriers from balance band into conduction band. This way the excited electrons gain enough kinetic energy to move freely and take part into conduction. These solid metals that conduct electricity are known as conductors and have the highest conductivity.

![Figure 2.4 Schematic diagram illustrating the energy-band formation](image-url)
2.3 Semiconductor Classification Based on Bandgap

Bandgap is the amount of energy required to stimulate an electron from VB to CB. There can be a different phenomenon when the plot is related between energy (E) and wave vector (k) which is shown in the following figure 2.5. Actually the electron momentum within a lattice structure is equivalent to the propagation constant (k) [40]. Brillouin zone is a very good parameter for characterizing the lowest and highest energy state in CB and VB respectively. Brillouin zone is basically a measure of momentum of a certain crystal. If the momentum of electrons and holes are equal in both the valence and conduction band, then the semiconductor is termed as a direct bandgap semiconductor.

The E-K diagram is shown in figure 2.5. All the photon must have a minimum energy equal to the bandgap for being promoted from valence band to conduction band and thereby get free to move within the lattice. The particle and wave nature of photon makes it very interesting in various research fields. Carrier generation and carrier recombination are two very common terms used in PV field. They are defined as the incident of exciting an electron by photon absorption and again the return of that excited electron to complete that vacancy respectively. The bandgap energy is very important as it is related to the wavelength of the emitted photon.
Figure 2.5 Illustration of (a) direct and (b) indirect bandgap semiconductor by E-K diagram [41]

On the other hand, indirect bandgap is somewhat complicated as it involves two particles for generation and recombination. These two particles are called photon and phonon and that’s why the probability of having both generation and recombination in indirect bandgap semiconductor is very low.

2.4 Methods for Porous Silicon Fabrication

When the silicon surface contains many pores or voids in the surface, then that silicon is referred to as porous silicon. Stain etching and electrochemical anodization are the two most popular procedures for fabrication porous silicon worldwide [42, 43].

The first method of stain etching uses a mixture of Hydrofluoric acid (HF) and Nitric acid (HNO3) which is a very powerful oxidizing agent. There is no application of external power supply in this method too. Most of the stain etching techniques are very simple and generate a coating of porous layer which is very thin in topography. However,
the greatest disadvantage of this method is that there are hardly any external experimental parameters which can be used for control of the pore characteristics and this is extremely important in case of porous silicon.

On the contrary, the electrochemical anodization technique is an extremely effective technique for the fabrication of porous silicon. As there are external experimental parameters involved in this method, so the pore characteristics can be effectively controlled in various ways leading to a large variety of thickness of the porous layer, pore thickness as well as pore diameters. This technique typically used an anodization cell containing the electrolyte and the counter electrode. The separation distance between the active electrode and the counter one is usually in the range of centimeters and external bias is also applied following different method of biasing.

2.5 Porous Silicon Formation

There are two basic chemical phenomena during the formation of porous silicon. The first step is called oxidation which is the incident of losing electrons. The second reaction is known as dissolution of silicon requiring holes in the valence band. That’s why during accumulation, oxidation automatically occurs for the p-type silicon whereas the n-type one requires an external illumination for the generation of holes finally moving to the depletion region area [44]. Quite a few techniques have been reported regarding the actual principle of pore formation in silicon as there is hardly any palatable clarification about it. The commonly accepted theory is that there is a gap necessity in the underlying oxidation ventures for both electro polishing and pore development [45]. Electronic property of the semiconductor such as band structure, type of dopants and the convergence of the dopants additionally decide the pore morphology [18]. The most
important parameters that affects the pore morphology are dopant concentration, concentration of fluoride ions in the electrolytic solution and the value of the applied electric field [44, 46].

At first, the silicon surface is passivated with hydrogen [47, 48]. One of the most established mechanism of chemical dissolution is described below [46, 49]. It clarified the advancement of hydrogen gas amid the procedure of electrochemical carving of silicon and opening prerequisite for the disintegration to happen which is acknowledged necessity [50] [18]. Another great part of this component is that it clarifies the fluoride debased hydride passivation layer as noticed quickly after anodization. The surface changes to oxide pollution once it is subjected to surrounding air [51, 52].

The synthetic equation of the first part of oxidation is as follows:

$$\text{Si} + 4\text{OH}^- \rightarrow 4\text{H}^+ + \text{SiO}_2 + 2\text{H}_2\text{O}$$

Then the chemical dissolution happens after the oxidation of Si per the following equations

$$\text{SiO}_2 \rightarrow 6\text{HF} + \text{H}_2\text{SiF}_6 + 2\text{H}_2\text{O}$$

So, the entire reaction results in

$$\text{Si} + 4\text{OH}^- + 6\text{HF} \rightarrow \text{H}_2\text{SiF}_6 + 4\text{H}_2\text{O}$$
The dissolution of the silicon surface is shown in by the following figure 2.6

Figure 2.6 Process-wise illustration of silicon anodization and dissolution [18]

Step 1: At first, hydrogen is soaked. Since the electron fondness of hydrogen is about that of silicon so the incited polarization amongst hydrogen and silicon molecule is not that high [44].

Step 2: Si-F bond reacts with the fluoride ion in a nucleophilic way when the hole moves into the silicon surface. The outcome is the formation of Si-F bond.

Step 3: Polarization impact will be brought about by Si-F bond that permits another fluorine particle to assault and supplant the hydrogen bond [46]. During this time, by infusing an electron into the substrate, two hydrogen atoms consolidate with each other.
Step 4: The electron thickness of the Si-Si back bonds diminishes in this manner to make them more inclined to react with fluoride particle. Therefore, outstanding silicon molecule on surface bonds to the hydrogen atoms. This is the final outcome of the polarization impacts of Si-F bond [53].

Step 5: The formed SiF$_6^-$ fluoroanion which is caused by the chemical reaction of silicon tetrafluoride is extremely stable. This process sustains until there is an availability of another positive charge carrier or hole.

2.6 Surface Topography of Formed Pores

The standards of porous structure classification are given by IUPAC (International Union of Pure and Applied Chemistry). On the basic of the diameter of pores (d), porous silicon is divided into three categories. The structures are called micropores (d>2nm), mesopores (d= 2-50 nm) and macropores (d>50nm) [18]. It lacks detailed explanation as it is only concerned with the pore diameter and disregards the morphology of the pores developed on the surface.

Pore morphology essentially deals with property like shape, introduction, interconnection of pores etc. The characterization in a systematic way becomes very tough as porous silicon contains a lot of details about pore morphology and pore distribution. Microporous and mesoporous silicon demonstrates a wipe like structure with thick and haphazardly stretched pores in a pore morphology. On the other hand, disjoint pores with short branches are typical properties of macroporous silicon [54].
2.7 Porous Silicon in PV Application

Porous silicon has been extensively used to increase the efficiency of Si solar cells. It mainly serves as an anti-reflection coating (ARC) and thereby trapping more light into the solar cell surface. As the output power is directly proportional to the input power in most of the circumstances, so the efficiency gets increased. The antireflection layer is the layer of dielectric that is coated on the surface of solar cell with the end goal that it reflects less light and there should be no absorbance. The main cause of the antireflection effect is due to the internal multiple reflection within the coatings and Air/ARC and ARC/substrate producing a destructive interference.

The figure 2.7(a) illustrate the Anti-reflection effect and figure 2.7(b) shows the structure of porous silicon. The range of interest for photovoltaic application lies within the 650nm-7500nm of wavelength. Reflection from both the top and bottom surface of the coating causing the destructive interference is the main source of the antireflection phenomenon. Constructive and destructive interference occurs when the phase shift between the reflected beams are 0° and multiples of 180° respectively [55] [56]. The amplitude between the multiple reflected beam and the air/ARC coating interface must be equal in value for the ARC layer to produce no reflectance within the wavelength of interest. This will be established when the refractive index, $n_1$ is equivalent to square root of the result of the refractive index of air ($n_0$) and index, $n_2$ of the substrate. Moreover, it has to be between the refractive index of air ($n_0=1$) and substrate, $n_2$ in the wavelength of interest [57, 58].
Figure 2.7 (a) Illustration of the antireflection coating and (b) cross-section view of the structure of porous silicon [59] [60]

\[ n_1 = \sqrt{n_0 n_2} \quad \ldots \ldots \ldots \ldots \quad (2.1) \]

The wavelength of the incident photon is much higher than the diameter of the pores. It can be said that silicon and air mixed together as a homogenous mixture is basically the porous silicon in terms of optics [61]. The refractive index of silicon (n_{c-si}) depends on the wavelength of light and it varies from 3.84 to 3.76 within the wavelength of interest from 650nm to 700nm respectively. Therefore, the refractive index of the ARC on top of the silicon needs to be equivalent to 1.96 and 1.94 at wavelengths of 650 and 700 nm individually. Porosity and refractive index, n_1 are related by the following equation [62]

\[ 1 - f_{air} = \frac{(1-n_1^2)(n_2^2 + 2n_1^2)}{3n_1^2(1-n_2^2)} \quad \ldots \ldots \ldots \quad (2.2) \]
Here $f_{\text{air}}$ represents the percentage porosity.

The governing equation to establish the second criteria is

$$d_1 = \frac{\lambda_{\text{min}} (1 + 2m)}{4n_1} \quad \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdOTS
For the electrochemical energy storage, the supercapacitor must have the electric-double-layer effect or the pseudo-capacitance effect. EDL occurs when the positively charged electrode have a layer of negative particles at the anode/electrolyte interface alongside a charge-adjusting layer of positive particles adsorbing onto the negative layer. The inverse is valid for the oppositely charged electrode. On the other hand, the effect of pseudo-capacitance takes place depending on the electrode material and surface shape, a few particles pervade the twofold layer ending up as adsorbed particles and contribute to pseudo-capacitance effect. This adds up to the aggregate capacitance of the supercapacitor. Both effects have been shown in figure 2.9(a) and 2.9(b).
2.9 Photoluminescence Spectroscopy of Porous Silicon

The luminescent property displayed by porous silicon has been the objective to manufacture porous silicon based light emitting diode (LEDs) incorporated on silicon chips. Photoluminescence (PL) shown by porous silicon is detectable at wavelengths ranging from bright (UV) [66] to the infrared area (IR) with excitation wavelength ranging between 260 nm (for UV outflow) and 520 nm [20]. Photoluminescence is straightforwardly identified with the electronic structure and movement. It is due to the radiative recombination of the transporters limited in nanoclusters of silicon installed into porous silicon layer [67, 68]. The correct component which portrays the photoluminescence property of porous silicon is still not accurately known. Several theory and models have been proposed [69]. It is trusted that quantum restriction assumes...
the key part [70]. As suggested by the quantum repression model, the small sized silicon branches contained in the porous silicon structure are subjected to quantum confinement and this results in photoluminescence [71]. High porosity silicon can be considered as a system of crystalline lattice having measurement in nanometer range and the quantum restriction in these one dimensional nanometer structures are in charge of extending the bandgap [20].

2.10 Raman Spectroscopy of Porous Silicon

The vibrational spectroscopy strategy to test the neighborhood nuclear course of action and vibrations is known as Raman spectroscopy. Different types of Raman scattering have been shown in figure 2.10. It has been utilized to describe the porous silicon [72] and silicon nanostructures [73]. To characterize the dimension of silicon crystallites, the maximum shift of one phonon and half width of crystalline silicon has been utilized frequently.

![Figure 2.10 Various types of Raman scattering during the Raman spectroscopy [74]]
The model (confinement of phonon) has been generally used to understand the Raman spectra of nanostructured semiconductor. The quantum control model was initially proposed by Rochester, Wang, and Ley [75, 76] combinedly called RWL model. Nanocrystalline silicon (Si) [73], Germanium (Ge) [77] and Gallium arsenide (GaAs) [78] contain peak shift, expansion, bond asymmetry and Raman spectroscopy has been very effective to explain all these.

2.11 Scanning Electron Microscope (SEM)

A device that utilizes highly energetic electron beam in place of the photons to produce an image of a sample is known as Scanning Electron Microscope (SEM) [79]. The imaging of the sample is done by raster scan pattern. Highly energetic electron beam shines on the surface of the specimen (conductive) bringing about dislodging of the electron from the valence shell. Signals delivered by the SEM are secondary electrons (SE) and back-scattered electrons (BSE). For the imaging, it is the identification of the back-scattered electron (BSE) by the identifier. Important properties regarding elemental composition, morphology of the intended surface as well as various other electrical properties can be gathered by the identification of the back-scattered electron (BSE). The basic construction of a SEM is shown in figure 2.11.
In SEM, highly energetic electron shafts are created from the thermionic discharge from the tungsten cathode. The screen monitor is the source of having the detection, process and collecting the actual image of the loaded sample of interest. SEM is extensively used for topographical characterization as it contains higher resolution and greater field depth in comparison to an optical microscope.

2.12 Electrochemical Characterization

2.12.1 Electrochemical Impedance Spectroscopy (EIS)

To analyze the electrochemical behaviors of any charge-storage device, the electrochemical impedance spectroscopy is the most commonly used measurement techniques. It is also referred to as an Alternating-Current (AC) impedance analyzer as it typically reveals various kinds of impedances related to the charge-storage device. It
usually contains much more detailed information than any single frequency measurement associated with Direct-Current (DC) techniques. There might be several reactions within the device and EIS measurement deals with indicating important information to differentiate among those experiments.

For performing the Electrochemical Impedance Spectroscopy (EIS) measurement, a voltage signal of sinusoidal nature is applied. The range of frequency of the signal is usually selected from KHz to mHz. The response is in the form of a plot and the impedance can be determined as each frequency and is also given directly by the curve itself. The resulting plot is the real impedance ($Z_{re}$) vs. the imaginary impedance ($Z_{im}$).

To discuss that what information can be extracted from an EIS plot, the nature of a standard EIS plot and the equivalent circuit of a supercapacitor is shown in the following figures 2.13 (a) and 2.13 (b) respectively. As seen from the equivalent circuit, figure 2.13 (b) consists of two resistances ($R_s$ and $R_{ct}$) and an electric double-layer capacitance ($C_{dl}$). $R_s$ represents the internal resistance of the whole device and it is connected in series with the parallel connection of $R_{ct}$ and $C_{dl}$. $R_{ct}$ is the charge-transfer resistance between the electrode-electrolyte interface and indicate the numbers of free slots for the adsorption of ions in the double layer and thereby hinting at the ionic resistance at the interface [7]. The $W_0$ in series with $R_{ct}$ is known as the Warburg impedance element and it represents the ionic nature of the device starting from the knee frequency and ending at the lower frequency which is indicated by the sharp spike in the EIS plot. The knee frequency is the end-point frequency of the semi-circle in the EIS plot. By determining the knee frequency, the electric double-layer capacitance ($C_{dl}$) can be calculated by using the following equation
\[ C_{dl} = \frac{1}{w Z_{im}} \] \[ \text{[81]} \] \[ \text{……………….. (2.4)} \]

Where, \( w = 2\pi f \)

\( f = \) knee frequency

\( Z_{im} = \) imaginary impedance corresponding to the knee frequency in the EIS plot

Figure 2.12 (a) the standard EIS plot and (b) the equivalent circuit of a supercapacitor \[ \text{[82]} \]

2.12.2 Cyclic Voltammetry (CV) Analysis

One of the most important potentiodynamic measurement involved in the electrochemical characterization of a device is the Cyclic Voltammetry (CV) analysis \[ \text{[83]} \]. This measurement basically involves the scanning of the active electrode in a linear way against the time. This significantly differs from the linear sweep voltammetry as there is one more scanning in the reverse way in case of CV. The scanning can be performed for as many cycles as needed and the cycle resulting in the best plot is taken
for analysis. The plot is a resulting curve of the current vs. the applied voltage and is commonly known as cyclic voltammogram.

The scan pattern between the voltage and time is linear and it can be continued to as many cycles as required in case of cyclic voltammetry measurement. The experimental scan rate (V/s) is defined as the rate of change of voltage per unit time [83]. The current versus the applied voltage is plotted. A gradually decreasing potential is applied in forward scan (from $t_0$ to $t_1$) and a current will flow in positive direction [83]. During the reverse scan (from $t_1$ to $t_2$), a current will flow in a negative direction if the redox coupling of the electrodes is reversible. The oxidation peak will follow a more similar pattern of the reduction peak if the redox coupling is as more reversible as possible. Thus, CV information can give data about redox possibilities and electrochemical response rates [83].

The applied voltage waveform (input) and the resultant standard cyclic voltammetry plot is shown in figure 2.13 and figure 2.14 respectively.
Figure 2.13 Input voltage waveform applied in Cyclic Voltammetry measurement [84]

Figure 2.14 Standard output plot from CV showing the peak cathodic and anodic current [85]
Chapter 3 Experimental Procedure

3.1 Fabrication of Porous Silicon

3.1.1 Substrate Cleaning

N-type single crystalline silicon substrate with (111) orientation was received and cut into 1 cm by 2 cm with diamond cutter. There is a high possibility of polluting the substrates while cutting, therefore they must be cleaned by a standard procedure.

All the diced samples were placed into a sample holder. Then, the samples were dipped into a container that contained soap water. The container was then put inside the ultrasonic bath for half an hour. Then the ultra-sonicated substrates were taken out from the soap water solution and rinsed with DI water for 10 minutes. The sample holder and the ultrasonic cleaner is shown in figure 3.1.
After that, the sample holder was dipped into a container having acetone. Acetone is a very effective chemical to remove the oil and other chemical residues from the surface of Si substrates. Then the container was again placed in the ultrasonic cleaner for 20 minutes.

The last step of cleaning was to clean these substrates with Isopropyl Alcohol (IPA) solution ultrasonically for 20 minutes. Then the substrates were dried out by the nitrogen-gas blower and preserved in a cleaned and large sample box.

3.1.2 Electrochemical Anodization

Electrochemical anodization technique was used to fabricate porous silicon. Anodization needs two electrodes to be used as anode and cathode. Silicon was anode and Pt was used as a cathode electrode during the experiment. The distance was
maintained at 1cm by tightening the screws of the electrode holder. There were two modes of operation to perform the electrochemical anodization. The two modes are called potentiostatic anodization and galvanostatic anodization. Potentiostatic and Galvanostatic anodization are also known as the Constant Voltage (CV) and Constant Current (CC) method respectively. The ultimate experimental set-up is shown in figure 3.2.

Figure 3.2 Experimental set-up of electrochemical anodization process

The CC method was performed using current densities of 10-50mA/cm² whereas the CV method was performed using voltages ranging from 20-90 volts. The electrolytic solution contained a mixture of ammonium fluoride (Acros organic), glycerol (fisher scientific), orthophosphoric acid (fisher scientific, 85%) and DI water. Two different beakers were used to prepare two separate mixtures. The first mixture contained 25 mL
of glycerol, 100 mL of DI water and at last 80 mL of orthophosphoric acid. The first mixture had a total volume of 205 mL. The second mixture contained 13 grams of crystalline Ammonium Fluoride and 25 mL of DI water. This mixture was stirred at 25°C for 40 minutes in a hot plate to properly dissolve the NH₄Fl powder in the water. Then another beaker was used to make the final electrolytic solution by taking 45 mL from the first mixture and 5 mL solution from the second mixture. So, the final solution had a total volume of 50 mL. The experiments were carried out in room temperature and normal humidity. All the volume measurements were done using beakers of appropriate size.

Several experiments were carried out both by CC and CV method. The power supply used was power supply (PAN 600-2A, Kikusui Electronics Corp.) which is a DC power supply. The time of anodization was varied between 5 minutes to 15 hours and room temperature was maintained during the experiments. After each experiment, the samples were rinsed with anhydrous alcohol and dried at room temperature.

3.1.3 Gold Deposition on Porous Silicon

The CrC-150 sputtering system shown in figure 3.3 was used to deposit a thin layer of gold on the porous silicon surface. At first, the system was switched on by pressing the power button in the back. Then the gas button using the 3-way manual selector was selected when the coat gas valve was set to zero. The coat gas control needle valve was rotated counterclockwise to increase the amount of argon gas. The pressure was set in the 2mTorr-5mTorr range and time could stabilize the meter from fluctuation. The time for stabilization was 2-3 minutes and is very much the same when the sputtering process is repeated. After that, the power control nob was first rotated anticlockwise and then it was rotated clockwise 5 times. This will make the output power almost 40 watts.
The desired thickness of the gold layer was 5nm. The plasma was started by pressing the process switch. After the desired thickness was achieved as seen in the thickness monitor, the process switch was turned off and the operation was repeated in a reverse way. The system was vented with air to open the chamber and collect the samples. This process was repeated for other porous silicon samples. All the samples were stored in a sample box for further experiment and analysis.

![Image of CRC-150 Sputtering system](image)

**Figure 3.3** Photograph of the CRC-150 Sputtering system used for gold-deposition

### 3.1.4 Supercapacitor Fabrication

At first, the fabricated samples were diced (1cm × 1cm) with a diamond cutter. Several samples were cut in this same dimension and were also labeled accordingly. After that, 1-2 drops of 1-Ethyl-3-Methylimidazolium Tetrafluoroborate (EMIBF₄, 97%, Sigma-Aldrich) was injected into the surface of the samples. This
electrolyte was used to create the electrode-electrolyte interface that produces the Electric-Double-Layer (EDL) effect. To infiltrate the electrolyte into the pores of the samples, the samples were loaded into a MTI vacuum oven and was sealed for two hours. After that, the samples were taken out from the vacuum oven and were carefully stored in a sample box to be used for electrochemical characterization later.

3.2 Scanning Electron Microscope

Scanning Electron Microscope (SEM) of the Hitachi S-3400N model shown in figure 3.4 was used to characterize the surface topography of the fabricated porous silicon samples. As usual, the samples were made conductive enough by attaching a carbon tape with them in the sample holder. The standard procedure of measuring the height and size of the stage and holder was followed before loading the sample inside the SEM. Different values of accelerating voltage were used for scanning and the values were varied between 5KV, 7KV and 10KV. Although various values were used, but 75% of the scanning was performed using the 10KV voltage as it produced the most stable images. The emission current during the scanning varied between 145 μA-150μA. The images were saved and then transferred to a compact disc from the computer for further analysis and comparison.
3.3 Optical Characterization

3.3.1 Reflectance

One of the most important purpose of this project was to reduce the reflectance loss. After fabricating porous silicon, the reflectance was measured using the Filmetrics software. This was established following some specified methods. At first, the fiber optic cable was connected in a proper way to the instrument to enable the reflectance measurement set-up. Then the light source was turned on and it was ensured that the device was switched on when the green LED was seen lit-up located in front of the Filmetrics. Then 5-10 minutes was the waiting time for warming-up the device and be ready for use. Bare Silicon-Di-Oxide (SiO₂) was used as the reference sample and was placed very carefully into the stage so that the light coming out from the device can shine
on the surface of SiO$_2$. Then the software film-measure was opened and after opening, the software itself gave some command windows regarding what to do. The baseline was created by measuring the reflectance of the reference SiO$_2$ sample. After that the porous silicon sample was loaded into the stage after taking out the reference sample. Then by using the software’s edit recipe button the proper recipe Si on SiO$_2$ was selected and the reflectance was measured by adjusting various parameters of the edit button. The measurement produced plots of the reflectance and they were saved as text files. Text files were transferred in a pen-drive to plot them in the origin software and analyze for results later. This process was repeated for each of the fabricated porous silicon samples made by CV and CC method.
3.3.2 Raman Spectroscopy

The Horiba Raman spectrometer shown in figure 3.6 was used for finding out the Raman shifts and thereby determining the materials present on the surface. The Raman spectroscopy was done following some specified steps. At first, by hitting the power button the green laser source was switched on and it was confirmed by the beep sound that it made while turning on. Then the objective lenses having 100 times magnification was calibrated with filter and grating of 0.6 and 1800 respectively.

The fabricated porous silicon samples were then put into the sample stage very carefully by using an IPA cleaned tweezer. The optical surface of the sample was very important as we need to focus on a region while doing Raman spectroscopy. To establish it, the Euromax device was switched on which was attached to the lenses stage. It was
required to focus the optical lenses as close as possible to the sample stage but not touching it. This was done very carefully with the help of a controlling stick. The lenses were moved very slowly until the expected surface was focused and seen on the screen of the computer monitor. After the desired surface was seen on the screen, the green laser was turned on after the light source of the Euromax device was switched off. After adjusting the Raman plots seen on the screen, the text file was transferred to a pen drive for further analysis and plotting.

Figure 3.6 Photograph of the Raman spectrometer set-up for Raman spectroscopy measurement

3.3.3 Photoluminescence Spectroscopy

The Edinburgh Xe-900 photoluminescence spectrometer shown in figure 3.7 was used to measure the photoluminescence properties of porous silicon. At first, the spectrometer was turned on by pressing five switches in ascending order written on each of the switches. Extreme care was maintained while putting the sample into the sample
holder inside the device as there was a high possibility of the sample falling inside the stage. The proper surface was also put on the top as it was required to focus on the porous surface of the loaded sample. The chamber door was closed after loading the sample inside. The software used for the PL measurement was Fe-900 and the initial excitation wavelength was around 450nm. The scanning was used to measure the emission between wavelengths ranging from 550nm to 8520nm. After getting the spectrum, the image files were saved as text files to further plot and analyze the data.

Figure 3.7 Photograph of the Edinburgh Xe-900 photoluminescence spectrometer

3.4 Electrochemical Measurements

3.4.1 Electrochemical Impedance Spectroscopy

The Celgard separator was used for this purpose. The separator was cut into pieces of similar size (1cm × 1cm) with the help of a hard paper and scissor. After that,
the pair of porous silicon sample were attached together and it was made sure that the separator was integrated properly by cutting the finer edges of it.

Two types of cells were used for the electrochemical measurements. The wafer cell was used primarily and then the sandwiched porous silicon electrodes were inserted into the coin cell to make a more compact contact and measurement. The VeraSTAT-3 instrument was used for the electrochemical measurements. After turning on the power button on the back of this device, the sandwiched electrodes comprising the wafer cell was connected to the cables which was coming out through the jack connected to the instrument. Then the VeraSTAT-3 software was opened in the computer integrated with the instrument. Then Potentiostatic EIS was selected from the toolbar of the opened window. The initial and final frequencies used were 100 kHz and 0.01 Hz respectively.

3.4.2 Cyclic Voltammetry Measurement

To measure the cyclic voltammetry characteristics of the wafer cell, the software was opened and CV measurement were selected from the “new experiment” tab. The measurement was alternatively done in single cycle and multiple cycles. After choosing the cycle, the initial and final potential was selected to be -1V and 1V respectively while the scan rate was alternatively varied between 0.02V/sec and 0.05V/sec.
Chapter 4 Results and Analysis

4.1 Characterization of Surface topography

4.1.1 SEM Images of Porous Silicon

Figure 4.1 (a) shows the SEM image of porous silicon fabricated by the 45V CV method. It is seen that the pores are quite clear and they have inconsistent size. Some pores are small whereas some others are bigger in size. Non-uniform size of the pores is attributed to the variable etching rate. Larger pores are formed at the beginning of the experiment which is attributed to the very fast etching rate. The smaller pores are formed at the later stages during the experiment when the etching rate slowed down significantly.

For an increased CV of 50 volts, the size of the pores got larger compared to the previous case as shown in figure 4.1(b) below. This was also accompanied by small pores inside some large pores throughout the surface. This can be attributed to the fact that some larger pores might contain a different lattice structure due to the difference in grain size. This in turn affects the etching rate which slows down as the time progresses and finally results in the smaller pores inside the larger ones. There were some individual small and large pores as expected for the 50V Potentiostatic anodization as well.
Figure 4.1 SEM image of porous silicon formed by Potentiostatic anodization (20 minutes) using anodization voltage of (a) 45V and (b) 50V.

So, it can be concluded that the pore size gets larger as the voltage is increased in case of potentiostatic anodization.

The SEM image obtained with the 10mA/cm² CC sample is shown below in figure 4.2 (a). The pores are very densely populated with the pores having the uniform size throughout the surface. This can be attributed to the fact that the etching rate is constant throughout the experiment. As the etching rate depends largely upon the variation in electric current, the etching rate doesn’t vary that much in this case of constant current anodization method. For the 20mA/cm² CC method, the sample contained bigger pore size and a non-uniform distribution of the pores within the surface. Very few tiny pores inside the larger pores were also observed and there were quite a few small pores as well.

This can happen when a larger value of current is used for a relatively longer period, the current tend to build up in a gradual way. Therefore, the etching rate varies
from the initial time to the final time which ultimately results in an inconsistent
distribution of the pore size. The formation of small pores within the large pores which
are very small in numbers is the result of the variation in grain size due to irregular lattice
structure of the larger molecules in the sample.

So, it can be concluded that the pore size gets larger as the current is increased in
the CC method to fabricate porous silicon samples.

Figure 4.2 SEM image of porous silicon formed by galvanostatic anodization (20
minutes) using anodization current density of (a) 10 mA/cm² and (b) 20 mA/cm²

Again to analyze the effect of the variation of time interval on pore characteristics
and for the simplicity of comparison and analysis, only 2 samples have been shown here.
The anodization time used for the samples were 10 minutes and 30 minutes. The samples
fabricated for 10 mins as shown in Figure 4.3(a) contains a uniform distribution of small
sized pores and the allocation is very densed. There are some void structures in the top
middle side of the image that indicates that there might not be any pores formed on those
places. This is in agreement with the theoretical concept as the etching rate is not constant throughout the experiment.

Similarly, the SEM image for the sample fabricated by the CV (90 volts) for 30 minutes has been shown in figure 4.3(b) below. This time, the pores are much larger in size and are very sharp and clear. The pores are attached to each other like a crystalline structure and the density of pores indicates a uniform distribution of the formed pores throughout the surface of the area of interest. The difference in pore-size can be attributed to the variable etching rate throughout the experiment.

So, it can be concluded that the increase in time results in an increase in the pore-size of the fabricated porous silicon samples.
4.1.2 Calculation of Porosity

The formed porous layer was removed by using the 3% KOH electrolytic solution and the mass was remeasured again after the porous layer was removed. Equation 4.1 below was used to calculate the porosity of the porous silicon samples.

\[
\text{Porosity (\%)} = \frac{(m_1 - m_2)}{(m_1 - m_3)} = \frac{(m_1 - m_2)}{(m_1 - m_2) + (m_2 - m_3)} \times 100\% \quad \text{(4.1) [30]}
\]

\(m_1\) = sample weight before anodization

\(m_2\) = sample weight after anodization

\(m_3\) = sample weight after removing the PS layer with KOH solution

The variation of porosity with the etching parameters is tabulated in table 4.1 and plotted in figure 4.4 respectively.
Table 4. Porosity for different etching parameters

<table>
<thead>
<tr>
<th>Etching Parameters</th>
<th>Voltage (V)</th>
<th>Current Density (mA/cm²)</th>
<th>Time (sec.)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>45</td>
<td>10</td>
<td>5</td>
</tr>
<tr>
<td></td>
<td>50</td>
<td>20</td>
<td>10</td>
</tr>
<tr>
<td></td>
<td>55</td>
<td>30</td>
<td>20</td>
</tr>
<tr>
<td></td>
<td>60</td>
<td>40</td>
<td>30</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th></th>
<th>Porosity (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage (V)</td>
<td></td>
</tr>
<tr>
<td>45</td>
<td>25.95</td>
</tr>
<tr>
<td>50</td>
<td>33.31</td>
</tr>
<tr>
<td>55</td>
<td>40.90</td>
</tr>
<tr>
<td>60</td>
<td>48.22</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Current Density (mA/cm²)</th>
<th>Porosity (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>5.17</td>
</tr>
<tr>
<td>20</td>
<td>9.43</td>
</tr>
<tr>
<td>30</td>
<td>14.31</td>
</tr>
<tr>
<td>40</td>
<td>20.07</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Time (sec.)</th>
<th>Porosity (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>7.83</td>
</tr>
<tr>
<td>10</td>
<td>14.28</td>
</tr>
<tr>
<td>20</td>
<td>71</td>
</tr>
<tr>
<td>30</td>
<td>59.87</td>
</tr>
</tbody>
</table>
Figure 4.4 Effect of variation of (a) voltage on porosity (b) current on porosity and (c) time on porosity
The above three plots shown in figure 4.4 depicts the relationship between the etching parameters and the porosity. It can be concluded from the results that each of the parameters affect the porosity linearly. This is also consistent with the SEM images as it was seen that the pore sizes got larger as each categories of the experimental anodization parameters got increased.

4.2 Optical Characterization of Porous Silicon

4.2.1 Reflectance Measurement of Porous Silicon

As shown in figure 4.5, all of the fabricated samples have reflectance less than 5% with one fabricated by the CV of 55volts having the minimum reflectance on an average throughout the spectral range of interest. This is around 8 times lower than the reflectance of the as received silicon sample which has a reflectance of more than 40% on an average.

The reflectance spectra for the 55V CV sample remains constant within the wavelength range (200nm-1600nm) whereas the 50V sample contains a very slow increase after the 1200nm of wavelength. The 45V sample has the maximum reflectance and remains fairly flat after the 400nm of wavelength while it has an inconsistent behaviour within the 200nm-400nm range of wavelength.

These measurements are quite consistent with the pore morphology as it was shown previously that the pore size gets bigger as the voltage gets increased for the CV method. Therefore, bigger pores trap more light and hence the reflectance gets much lower and lower. That’s why the 55V sample has the minimum reflectance and the 45V
sample produces the maximum.

![Image of reflectance comparison graph]

Figure 4.5 Reflectance comparison of porous silicon samples fabricated by different values of anodization voltages

The reflectance of the fabricated samples made by the CC method were measured in a similar way. All the samples were fabricated using the constant time of 30 minutes and the 3 samples that have been shown here in figure 4.6 have an galvanostatic current density of 10mA/cm², 20mA/cm² and 30mA/cm² respectively.

Again, this measuremnt was done to see how does the current density affects the reflectance measurement as it produced differnet pore morphology with the variation in current density already shown in the earlier section of SEM image analysis.
All of the samples exhibited reflectance less than 5% again which is 8 times lower than that of the as received silicon sample. The sample fabricated by the 30 mA/cm\(^2\) current density has the lowest reflectance that produced almost a flat pattern throughout the wavelength of interest (200nm-1600nm).

The porous silicon sample fabricated by the 20mA/cm\(^2\) current density showed a gradual increase after the 800nm of wavelength whereas it remained fairly constant within the 200nm-800nm wavelength range. The highest reflectance was produced by the sample fabricated by the 10mA/cm\(^2\) CC method and exhibited slow linear increase with the increase in wavelength.

As concluded in the previous section, these results are again supportive of the fact that the pore size gets larger as the current density is increased. As a result, the bigger pore traps more light thereby reducing the reflectance significantly.
Finally, the reflectance was measured for the anodized sample prepared by different anodization time. The reflectance spectra for the 10 minutes and 30 minutes anodized sample is shown in figure 4.7 and figure 4.8 respectively.

The reflectance is lower for the 30 minutes anodized sample fabricated by the 90V CV method compared to the 10 minutes anodized sample. For the 10 minutes porous silicon sample, most of the area within the surface have an average reflectance of 5% whereas for the 30 minutes sample the reflectance is 3% on an average. This is attributed
to the fact that the larger pores tend to trap more light as the time increases the pores get larger as seen in by the SEM analysis in the previous section.

Figure 4.7 Reflectance spectra for porous silicon sample fabricated for 10 minutes of anodization for three different regions (region-1, region-2 and region-3)
Figure 4.8 Reflectance spectra for porous silicon sample fabricated for 30 minutes of anodization for three different regions (region-1, region-2 and region-3)

The variation of reflectance with the variation of different anodization parameter is summarized in figure 4.9 below.
4.2.2 Photoluminescence Properties of Porous Silicon Samples

All the fabricated samples had the photoluminescence property as shown in figure 4.10 and figure 4.11 for the potentiostatic and the galvanostatic anodized samples.
respectively. The 45V anodized sample (black marked) contained PL spectra from low intensity to high intensity within a wavelength range of 540nm-800nm. The peak position of the PL spectra was at 675nm. Both the 50V (red-marked) and 55V (blue-marked) anodized samples had lower intensity compared to the 45V one and the intensity was constant throughout the wavelength. The 50V anodized sample exhibited two peaks at around the wavelength of 575nm and 660nm whereas the 55V anodized sample had one PL peak at 670nm. The variation of PL peak was not constant with the nature of the pores and this needs further investigation.

In the same way, the 40mA/cm² anodized samples (blue-marked) exhibited variation from lower intensity to higher intensity within the wavelength range of 500nm-800nm. The maximum peak intensity occurred at 670nm. The 30mA/cm² anodized sample (red-marked) had very low intensity throughout the wavelength range and PL peak was observed around 650nm. The 20mA/cm² anodized sample also showed very low intensity with a peak intensity at 540nm of wavelength. Again, in this case, the variation of PL intensity was not consistent with the nature of the pores and this needs further investigation.
Figure 4.10 Photoluminescence spectra of porous silicon samples formed by CV method of anodization

Figure 4.11 Photoluminescence spectra of porous silicon samples formed by CC method of anodization
4.2.3 Raman Analysis of Porous silicon

In order to find whether there are other materials present in the fabricated porous silicon surface, Raman spectroscopy was performed for all the samples. Figure 4.12(a) and 4.12(b) shows the surface topography obtained during the Raman spectroscopy.

Figure 4.12 Surface topography obtained during Raman spectroscopy for porous silicon samples prepared using anodization voltage of (a) 45V and (b) 50V

Figure 4.13 shows the Raman spectra of the porous silicon samples fabricated by the 45V and 50V CV method along with that of the as received silicon wafer. The non-anodized silicon wafer had a peak around 520cm whereas the anodized samples exhibited a very small shift in the left from 520cm. The peak was broadened for the as received silicon wafer whereas the anodized samples has a very short and sharp peak. Also, the anodized samples broadened more on both sides of peak extending to both the lower and higher frequencies compared to the as received silicon sample which had a lower extension of the peak on both sides.
As all the peaks for the Raman shifts lies around 520cm\(^{-1}\), so it can be concluded that only Si was present on the surface of the pores and that is what we expect from our experiment.

![Raman spectra of porous silicon samples fabricated by different values of voltage](image)

**Figure 4.13** Raman spectra of porous silicon samples fabricated by different values of voltage

Similarly, Raman spectra was carried out for the porous silicon samples fabricated by the Galvanostatic (CC) anodization. Figure 4.14(a) and 4.14(b) respectively shows the surface topography of the porous silicon samples fabricated by using two different anodization current density.
Figure 4.14 Surface topography obtained during Raman spectroscopy for porous silicon samples using current density of (a) 30mA/cm² and (b) 40mA/cm².

The samples tested were fabricated by the CC method using the current density of 30-50mA/cm² with an increment of 10mA/cm². The Raman plot is shown in figure 4.15. As seen previously, these samples have Raman shifts of around 520cm⁻¹ which is the standard Raman shift for the porous silicon sample.

In conclusion, it can be said that the porous silicon samples have only silicon on the surface when fabricated by the CC method and this is expected as well.
4.3 Supercapacitor Characteristics of Porous Silicon

4.3.1 Electrochemical Impedance Spectroscopy (EIS) Analysis

The EIS of the porous silicon samples fabricated by the 50V Potentiostatic anodization method has been shown in figure 4.16. It is seen that the charge-transfer-resistance ($R_{ct}$) is almost $2M\Omega$ which is a very high number. The higher value of $R_{ct}$ can be attributed to the fact that there is an oxidation of the Si with the electrolyte. That’s why it loses electron and thereby acting as nearly an insulator in this case indicating that the capacitor cell has a very poor ionic conductivity between the electrode-electrolyte interfaces. As discussed earlier, this accounts for the parallel resistance with the double-layer capacitance.
The higher value of $R_{ct}$ also indicates that there are very few available slots for the adsorption of ions in the double layer which ultimately results in a very high value of the ionic resistance at the interface. This in turn results in a larger semicircle seen in the Nyquist plot shown in figure 4.16.

After the semicircle portion, the slope of the impedance is linear and that results in a very low value of the Warburg impedance element ($W_0$) which is $\sim 0.303\text{nS}$. This lower value of $W_0$ is an indication of the fact that the diffusion of ions from the electrolyte to the pores is very inefficient resulting in poor capacity of the device to store charge.

Finally, the electric-double-layer capacitance ($C_{dl}$) was calculated by using equation (2.4) which gave a value of $0.3\text{nF/cm}^2$ and $6\text{nF/cm}^2$ respectively for the two semicircles using the knee frequency of 58Hz and 23Hz respectively. This indicates that the overall capacitance is the contribution of two electrode-electrolyte identical interfaces within the device.
Similarly, the EIS spectroscopy was performed for the porous silicon sample fabricated by the CC (10mA) method which is shown in figure 4.17. There is only one semicircle indicating only one electrode-electrolyte interface which contributes to the overall double-layer capacitance.

The summary of the other values of $R_{ct}$, $C_{dl}$ and $W_0$ have been tabulated in Table 4.2 for both the samples fabricated by CV and CC method.
Figure 4.17 EIS spectroscopy showing the Nyquist plot of the PS sample fabricated by the CC (10mA) method

Table 4. Parameters calculated from EIS spectroscopy for the porous silicon

<table>
<thead>
<tr>
<th>Parameters from EIS</th>
<th>Uncoated PS (CV-45V)</th>
<th>Uncoated PS (CC-10mA/cm²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{ct}$ (Ω)</td>
<td>1.8M</td>
<td>400k</td>
</tr>
<tr>
<td>$C_{DL}$ (nF)</td>
<td>0.3</td>
<td>3.79</td>
</tr>
<tr>
<td></td>
<td>6.0</td>
<td></td>
</tr>
<tr>
<td>$W_0$ (nS)</td>
<td>0.303</td>
<td>384.62</td>
</tr>
</tbody>
</table>
4.3.2 Cyclic Voltammetry (CV) Analysis of Porous Silicon

The CV plot using a scan rate of 0.2V/sec of the supercapacitor device made by the pair of porous silicon samples fabricated by the 45V potentiostatic anodization has been shown in figure 4.18. The electrochemical window is very narrow and the loop ends before reaching the ending voltage of -1V. The symmetric current is about 0.5nA which is very low.

These results can be attributed to the fact that the electrode-electrolyte surface takes part in reaction and thus the active material (silicon) is converted into silicon-dioxide (SiO₂). Therefore, the electrochemical window is very scattered ending before the ideal loop condition. The lower value of the current is because the interface is almost like an insulator with extremely high resistance as discussed in the previous section of the EIS plot.
Similarly, the CV plot using a scan rate of 0.2V/sec of the porous silicon sample made by the supercapacitor device fabricated by the Galvanostatic anodization (10mA/cm²) has been shown in figure 4.19. The electrochemical window is a bit bigger compared to the previous sample but it shows the same scattered properties as the loop ends before reaching the ending voltage of -1V. The value of the symmetric current is ~100nA and this high value can be attributed to the extensively resistive electrode-electrolyte interface of the sample.
Overall, both the CV plots of the porous silicon samples agree with their respective Nyquist plots. These results bear evidence that the porous silicon samples might not be a good electrode for fabricating supercapacitor and further surface engineering is necessary to improve the performance.

![Figure 4.19 CV measurement of supercapacitor cells fabricated using PS cells prepared by Galvanostatic (10mA/cm²) method](image)

4.4 SEM Analysis of the Passivated (Gold-Deposited) Porous Silicon Samples

To prevent the oxidation of the silicon in the interface, the porous silicon samples were passivated by depositing a thin layer of Gold (Au) using the sputtering method of deposition. To survey the surface topography after the deposition, the SEM imaging was
performed on the samples. The SEM images of the porous silicon samples (fabricated by 10mA/cm² Galvanostatic anodization) after Au deposition is shown in figure 4.20.

Figure 4.20 SEM image of porous silicon sample (10mA/cm²) after passivated by gold sputtering

The thin gold layer of 5nm thickness has covered the porous silicon surface blocking some of the smaller pores which was dominating the surface before this thin layer of coating. The pore sizes have got smaller and the distribution of the pores are somewhat uniform throughout the surface. In some areas, the smaller sized pores got fully covered by the gold layer whereas the relatively larger pores are quite clearly seen in the surface. The clearly visible area containing yellow marks indicate the surface having gold deposition which is extensively distributed throughout the surface. In short, the gold coating doesn’t block all the pores as it is a very thin layer and its purpose is to
passivate the porous silicon surface to prevent it from oxidation effect while integrating the porous silicon samples to make a supercapacitor device.

4.5 Supercapacitor Characteristics of Passivated Samples

The EIS and CV plots for the supercapacitor cell made by the pair of the passivated porous silicon samples fabricated by the Galvanostatic anodization (10mA/cm²) method was again performed. The figures are shown in figure 4.21 and figure 4.22 respectively.

As seen by the Nyquist plot, there is only one semicircle after the surface passivation indicating that the electric-double-layer capacitance is produced by only one interface. The charge-transfer resistance (R_{ct}) is now reduced to almost 40Ω which is extremely lower than the supercapacitor device integrated by the un-passivated pristine porous silicon samples fabricated by the same parameters of the anodization method. This is mainly due to the passivation of the Si surface which inhibits it to react with the liquid electrolyte and thereby the active material Si does not get oxidized.

The electric double layer capacitance is also increased drastically because of the low imaginary impedance produced on the knee frequency. The Warburg impedance element (W_0) is also increased indicated by the flat linear slope of the Nyquist plot after the semicircle portion. This means that after surface passivation, there are plenty of available slots for the efficient diffusion of ions into the pores and thereby enabling the device to store more charge.

The Cyclic Voltammetry (CV) plot shown in figure 4.22 exhibits a larger electrochemical window than the previous one and the symmetric current is about ~1µA
which is 500 times greater than the previous supercapacitor device made with pristine porous silicon samples. The double-hoop during both the cycles that diverges the curve to a non-ideal loop is attributed to the fact that the oxidation may not be completely prevented by the coated gold layer. Furthermore, the oxidized Si is not uniformly distributed throughout the surface and the crystal lattice can be considered as a structure containing a sequence of defects [25].

In addition, when the porous layer is being stabilized by water after the electrochemical etching solution is removed, there is chance of further dislocations within the porous structure. All these factors give rise to the fluctuated loop in the CV plot and hence the curve differs a bit from the ideal loop trajectory.

Figure 4.21 Nyquist plot of the supercapacitor device fabricated by using passivated porous silicon samples (10mA/cm²)
In the same way, the pair of passivated samples fabricated by the Potentiostatic anodization were again used to make the supercapacitor device. The EIS and CV plots are shown in figure 4.23 and figure 4.24 respectively.

As seen in the figure 4.23, the EIS plot contains two semicircles suggesting that the overall electric double-layer capacitance is an outcome of the two electrode-
electrolyte interfaces. There is also huge improvement in all the parameters such as charge-transfer resistance ($R_{ct}$), Warburg impedance element ($W_0$) and the double-layer capacitance ($C_{dl}$). The results of both the passivated supercapacitor devices have been summarized in Table 4.3.

Figure 4.23 Nyquist plot of the supercapacitor device fabricated by using passivated porous silicon samples (45V)
Figure 4.24 CV plot of the supercapacitor device fabricated by using passivated porous silicon samples (45V)
Table 4. 3 Parameters calculated from EIC spectroscopy for the passivated porous silicon supercapacitors

<table>
<thead>
<tr>
<th>Parameters from EIS</th>
<th>Passivated PS (CV method)</th>
<th>Passivated PS (CC method)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{ct}$(Ω)</td>
<td>1700</td>
<td>43</td>
</tr>
<tr>
<td>$C_{DL}$(nF)</td>
<td>4.97</td>
<td>371.1</td>
</tr>
<tr>
<td></td>
<td>16.5</td>
<td></td>
</tr>
<tr>
<td>$W_0$ (mS)</td>
<td>1</td>
<td>27</td>
</tr>
</tbody>
</table>
Chapter 5: Summary and Conclusions

5.1 Summary

The demand of electrical energy as well as electrochemical energy storage is an ever-increasing phenomenon. The production of electrical power is mostly carried out through non-renewable energy sources which are extremely harmful for the environment and the living beings. Therefore, solar cells can be an effective alternative to meet the goals of producing electrical power from sunlight without producing harmful effects to the environment.

To reduce the reflection loss, silicon surface can be made to have a porous structure which will enable it to trap more incoming light into the pores. This will result in more trapping of the sunlight and thereby reducing the reflection loss and finally increasing the solar cell efficiency.

There were basically two major objectives of this research project; the first one was to effectively control the pore morphology using the etching parameters of the anodization procedure. The second objective was to fabricate supercapacitors by a little bit of surface engineering on the produced porous silicon surface.

The \( \text{NH}_4\text{Fl} \) electrolytic etching solution can be the most efficient one to carry out the electrochemical anodization procedure for fabricating porous structure. This solution is extremely benign, offers flexible control of the porous structure by controlling the etching parameters during the experiment and the reflectance can be reduced drastically by fabricating porous silicon samples using this method of anodization.
As received silicon samples were cut into a proper size to be used in the electrochemical anodization technique. The electrolytic solution was prepared using a mixture of ammonium fluoride (Acros organic), glycerol (fisher scientific), orthophosphoric acid (fisher scientific, 85%) and DI water. The diced silicon samples were used as the active electrodes (anode) whereas the Pt foil of the same size as silicon was used as the cathode.

The analysis of SEM imaging was done and it was found that the pore morphology has a linear relationship with the etching parameters. As all the etching parameters (voltage, current and time) were increased, the size of the pores got larger and vice-versa. Then the reflectance was measured using the Filmetrics and almost all the samples produced reflectance less than 5% on an average. The thickness of pores was calculated using the weight loss method and it was consistent with the surface topography exhibited by the SEM images of the samples. From this analysis, it was concluded that the porous structure can be effectively controlled by the variation of the etching parameters (voltage, current and time) and hence the reflectance can be effectively reduced.

To survey the supercapacitor properties of the fabricated samples, a pair of samples having the same etching parameters were sandwiched together with a separator (celgard, dipped into the EMIBF4 electrolyte) in between to make a capacitor like structure. This process was repeated to make several such supercapacitor devices using different samples fabricated by the methods of Potentiostatic anodization and Galvanostatic anodization technique. After performing the EIS and CV spectroscopy of these supercapacitor devices, it was seen that, due to the oxidation effect, it produces a
very high value of the charge-transfer resistance which in turns produce a very low value of the overall capacitance.

To improve the capacitance, the fabricated porous silicon samples were sputtered by Gold (Au) to have a very thin layer of gold coating into the surface. The main purpose of this sputtering technique was to passivate the surface and prevent the oxidation of the active material Si in the electrode-electrolyte interface.

5.2 Conclusions

The method of electrochemical anodization using the NH$_4$Fl electrolytic etching solution was extremely benign, cost effective and offered flexible control of the pore morphology. The porous silicon samples were efficiently fabricated using this method and the pore morphology and structure were effectively controlled by controlling the various etching parameters of the experiment. It was found that the porosity and diameter have almost a linear relationship with the etching parameters. As the etching voltages, currents and time were increased, the thickness of the fabricated pores also increased and vice-versa. One of the exceptions was that the optimum time for the maximum porosity was 20 minutes rather than any greater time which required further investigation. The reflectance was drastically reduced to less than 5% for all the fabricated samples which was one of the basic goals of this project to make it more applicable and efficient to be used as an antireflection coating for more efficient silicon solar cells. The supercapacitor devices fabricated by different porous silicon samples yielded better results when the porous silicon surface was passivated by a thin layer of gold deposited by the sputtering process and was integrated in a coin cell rather than the wafer cell itself. The supercapacitor device made by the passivated porous silicon samples resulted in a charge-
transfer resistance \((R_{ct})\) of 43Ω, a Warburg impedance element \((W_0)\) of 27mS and an electric double-layer capacitance \((C_{dl})\) of 371.17nF which results in an improvement of \(~9302\) times of \(R_{ct}\), \(~97.88\) times of \(C_{dl}\) and \(~70\) times of \(W_0\) compared to the pristine porous silicon samples.

5.3 Future Tasks

The future work should include: 1) the effect of pore morphology on the photoluminescence spectroscopy 2) further investigation into the effect of time on porosity and 3) use of other materials to passivate the surface for better results of supercapacitor performance.
References


[34] "Intrinsic carrier concentration in semiconductors," ed.


[36] "Intrinsic Semiconductor," Available: [http://hyperphysics.phy-astr.gsu.edu/hbase/Solids/intrin.html#c1](http://hyperphysics.phy-astr.gsu.edu/hbase/Solids/intrin.html#c1)

[37] "n-type doping," F. c. o. semiconductors, Ed., ed.


[56] "Constructive and Destructive Interference," Available: [http://www.phys.uconn.edu/~gibson/Notes/Section5_2/Sec5_2.htm](http://www.phys.uconn.edu/~gibson/Notes/Section5_2/Sec5_2.htm)


