The Field-effect Transistor as a Mixer

Garald C. Sundberg

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THE FIELD-EFFECT TRANSISTOR AS A MIXER

BY

GARALD C. SUNDBERG

A thesis submitted in partial fulfillment of the requirements for the degree Master of Science, Department of Electrical Engineering, South Dakota State University 1968

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Thesis Adviser Date

Head, Electrical Engineering Department Date
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Since the advent of the superheterodyne receiver, the signal mixer has been an important part of the communications receiver. A signal mixer is a circuit that combines signals at two frequencies in order to transpose information from a high frequency to a lower frequency. The frequency conversion process permits amplification at a relatively low frequency where high selectivity and high gain can be more easily obtained.

Mixing may be visualized as a modulation process in which the amplitude of one signal is made to follow the variations of another signal. This process produces two new frequencies which are the sum and difference frequencies of the incoming signals.

Because the mixer is located in the small-signal front end of a receiver, its operation determines the sensitivity and selectivity of the receiver. Sensitivity is determined by the amount of noise generation in a receiver, and selectivity depends on intermodulation distortion and cross-modulation distortion. These factors are all important considerations in the design of a mixer.

The vacuum tube, transistor, and diode are common devices used for mixing. Within the last few years a new active device, the field-effect transistor, has shown great promise as an electric component. The field-effect transistor is known to exhibit properties of low noise, high gain, and, because of its square-law transfer characteristics, low cross-modulation distortion.
The objective of this dissertation is to analytically and experimentally investigate the field-effect transistor as a mixer. The areas of study undertaken are:

1. Analysis of the parameters affecting mixing action.
2. Static-bias potentials for optimum mixing.
3. Conversion noise figure. This area also involves the correlation between amplifier and mixer noise factors.
5. High frequency mixing.
CHAPTER 1

THE FIELD-EFFECT TRANSISTOR

In recent years the field-effect transistor (FET) has emerged as an important device in the field of electronic components. The FET has in fact been found to be superior to both the vacuum tube and the bipolar transistor in many of its characteristics. Its superior properties include high input impedance, low noise and very low cross-modulation distortion. The two basic types of FET's on the market today are the junction type (JFET) and metal-oxide-semiconductor type (MOSFET). The latter is also referred to as the insulated-gate FET. A list of important FET parameter symbols and definitions are provided in Table 1 on page 9.

The FET operates on the principle that the conductance of a channel of semiconducting material can be modulated or regulated by the magnitude of an input voltage. The signal input to the device is applied to a reversed-biased p-n junction. Output current flows through a bar or channel of p-type or n-type material; not through a junction as in the conventional transistor.5

Figures 1 and 2 show a sectional view of an n-channel FET along with its symbol and biasing arrangement. The terminals are referred to as gate, source, and drain. The gates are normally connected internally. However, they can be separated to provide independent control of the channel current.
Fig. 1.
Sectional view and circuit diagram for n-channel junction FET

Fig. 2.
Biasing for n-channel junction FET
The junction FET is a normally "on" device; the conducting channel connects the source to the drain even in the absence of gate-to-source voltage. For the n-channel FET, a negative gate voltage depletes the channel of carriers and thus lowers channel current. A positive gate voltage is required to reduce the channel current of the p-channel FET. The voltage applied between the gate and the source that reduces the channel conduction to zero is called the pinch-off voltage, $V_P$. For gate voltage ($V_{GS}$) greater than $V_P$ the only d.c. currents that flow are the reverse-saturation-leakage currents $I_{DS0}$ and $I_{SS0}$.

The channel conductance $g_{ds}$ may be increased by forward biasing the gate with respect to the source (Fig. 3). This usually isn't done because the gate-to-channel current rises exponentially when forward biased.

Common-source output and transfer characteristics of a typical n-channel FET are shown in Figure 4. In the low-current region, the drain current is linearly related to $V_{DS}$. As $I_D$ increases the channel begins to deplete and the slope of the $I_D$ curve decreases. At ($V_{DS} = V_P$), $I_D$ "saturates" and stays relatively constant until avalanche breakdown is reached. The avalanche breakdown, known as $BV_{DSS}$, is a reach-through effect from the drain to the source. Normal operation is with $V_{DS}$ above pinch-off ($V_P$) and below avalanche breakdown. In this active region the device provides high gain and large output impedance.
Fig. 3. Dynamic conductance curves versus gate voltage for junction FET.

Fig. 4. (a) Output, (b) Transfer characteristics of a typical FET.
The most important parameter used in describing FET operation is transconductance. Mathematically,

\[ g_m = \lim_{V_{GS} \to 0} \frac{\Delta i_D}{\Delta V_{GS}} \bigg|_{V_{DS} = \text{Const.}} = \frac{i_D}{V_{GS}} \bigg|_{V_{DS} = \text{Const.}} \]  

(1-1)

This parameter is also referred to as \( g_{mo} \), \( g_{fs} \), and \( \mu_{fs} \). Typical values of \( g_m \) lie between 500 and 10,000 \( \mu \)mhos. Other important parameters are listed in Table 1.

The small-signal common-source equivalent circuit is shown in Figure 5. This circuit shows that the input is essentially capacitive, that the output current is a function of the input voltage, and that the load is shunted by the output conductance and capacitance of the device.

At low frequencies, one may neglect the capacitive effects and assume that the input impedance is infinite. This results in a simplified expression for common-source voltage gain:

\[ A_V = \frac{v_{out}}{v_{in}} = -g_m (R_L || r_{ds}) \]  

(1-2)

or

\[ A_V = -g_m \frac{R_L r_{ds}}{R_L + r_{ds}} \]  

(1-3)

Note that the common-source configuration provides phase reversal not present in other FET connections.

The metal-oxide-semiconductor FET (MOSFET) is similar to the junction FET. An important difference between it and the JFET is that the gate is insulated from the channel by an oxide dielectric. The
gate can therefore be forward biased to enhance the channel as well as reversed biased to deplete it. The insulated gate construction also exhibits a much greater input impedance than the junction FET.

Fig. 5. FET small-signal common-source equivalent circuit.
### Table I

**IMPORTANT FET PARAMETERS**

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<th>Parameter</th>
<th>Meaning</th>
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<tr>
<td>$B_{V_{GS}}$ or $B_{V_{GDS}}$</td>
<td>Breakdown voltage from gate-to-channel with gate junction reversed-biased.</td>
</tr>
<tr>
<td>$B_{V_{DGO}}$ and $B_{V_{SGO}}$</td>
<td>Similar to the above except that either source ($B_{V_{DGO}}$) or drain ($B_{V_{SGO}}$) is open-circuited.</td>
</tr>
<tr>
<td>$B_{V_{DS}}$ or $B_{V_{DGS}}$</td>
<td>Breakdown voltage from drain to source with $V_{GS} = 0$.</td>
</tr>
<tr>
<td>$I_{GSS}$, $I_{DGO}$ and $I_{SGO}$</td>
<td>Gate-leakage current (gate to channel in junction FET's, gate to body in MOS); leakage current from drain ($I_{DGO}$) or source ($I_{SGO}$).</td>
</tr>
<tr>
<td>$I_{DSS}$</td>
<td>Drain to source current with $V_{GS} = 0$.</td>
</tr>
<tr>
<td>$I_D$</td>
<td>Drain current under specified conditions.</td>
</tr>
<tr>
<td>$I_{D(OFF)}$ and $I_{S(OFF)}$</td>
<td>Drain or source current with channel current cut off. $V_{GS} &gt; V_p$.</td>
</tr>
<tr>
<td>$V_{GS}$</td>
<td>Gate to source voltage under specified conditions.</td>
</tr>
<tr>
<td>$V_p$</td>
<td>Gate pinch-off voltage. The gate voltage that reduces the drain current to essentially zero.</td>
</tr>
<tr>
<td>$g_{fs}$ or $</td>
<td>g_{fs}</td>
</tr>
<tr>
<td>$S_{ds}$</td>
<td>Dynamic drain-source (channel) conductance.</td>
</tr>
<tr>
<td>$r_{DS}$</td>
<td>Static drain-source resistance.</td>
</tr>
<tr>
<td>$C_{gd}$</td>
<td>Small-signal, common-source, short-circuit reverse transfer capacitance.</td>
</tr>
<tr>
<td>$C_{gs}$</td>
<td>Small-signal, common-source, gate to source capacitance.</td>
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CHAPTER 2

NONLINEAR BEHAVIOR OF FIELD-EFFECT TRANSISTORS

Mixing in any device is accomplished as a result of a nonlinearity, principally of a square-law nature. Consider a square-law characteristic such as

\[ i_d = k \cdot v_{gs}^2 + k \cdot v_{gs} \]  \hspace{1cm} (2-1)

Let us assume that \( v_{gs} \) represents the sum of two sinusoidal waveforms \( V_{RF} \sin \omega_{RF} t + V_{LO} \sin \omega_{LO} t \). The squaring of this sum in Equation (2-1) will yield:

\[ i_d = k \cdot v_{gs}^2 = k \left( V_{RF} \sin \omega_{RF} t + V_{LO} \sin \omega_{LO} t \right)^2 \]

\[ = k \left( V_{RF}^2 \sin^2 \omega_{RF} t + 2 V_{RF} V_{LO} \sin \omega_{RF} t \sin \omega_{LO} t + V_{LO}^2 \sin^2 \omega_{LO} t \right) \]

\[ = k \frac{V_{RF}^2}{2} \left( 1 - \cos 2 \omega_{RF} t \right) + k V_{RF} V_{LO} \cos (\omega_{LO} - \omega_{RF}) t \]

\[ - k V_{RF} V_{LO} \cos (\omega_{LO} + \omega_{RF}) t + k \frac{V_{LO}^2}{2} \left( 1 - \cos 2 \omega_{LO} t \right) \]  \hspace{1cm} (2-2)

The terms normally of interest in a mixer are the sum and difference frequency terms \( \omega_{LO} \pm \omega_{RF} \). In most cases the intermediate frequency (IF) is the difference frequency.

Because mixing is dependent upon a nonlinearity, we shall study the nonlinear areas of the FET characteristics, and evaluate the areas of nonlinearity with respect to mixing action.
Richer and Middlebrook\textsuperscript{10} have reported the transfer characteristics for the junction FET in the pinched-off region to be described by the power-law relation

\[ I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P} \right)^n \]  \hspace{1cm} (2-3)

with

- \( I_D \) = static drain current,
- \( I_{DSS} \) = static drain current with zero gate-source voltage,
- \( V_{GS} \) = static gate-source voltage, and
- \( V_P \) = pinch-off potential.

Experimental work by Sevin shows that the exponent \((n)\) equals 2 for most common FET types.\textsuperscript{13} Equation (2-3) represents a nonlinearity within the \( I_D - V_{GS} \) plane.

There are at least five other areas of nonlinearity exhibited by the FET.\textsuperscript{3}

1. At values of \( V_{DS} \) below pinch-off. Here the device essentially shifts from pentode-like characteristics to triode-like behavior. This type of behavior is not predicted by Equation (2-3). (This is also true of many of the other nonlinearities.)

2. In the "cutoff" area. Here \( V_{GS} \) approaches \( V_P \) and the transconductance approaches zero.

3. In the "saturation" region with \( V_{DS} \) below pinch-off.

4. At the input junction. This occurs when the junction becomes forward biased by the input signal.

5. At breakdown of the gate-drain diode. This represents one of the more abrupt forms of nonlinearity.
Let us first assume that the FET characteristics are completely predicted by the power-law relation.

\[
I_D = I_{DSS} \left( 1 - \frac{|V_{GS}|}{|V_P|} \right)^2
\]  
(2-4)

The slope of this curve is the small-signal transconductance, \( g_m \):

\[
g_m = \frac{\partial I_D}{\partial (V_{GS})} = \frac{2I_{DSS}}{|V_P|} \left( 1 - \frac{|V_{GS}|}{|V_P|} \right)
\] 
(2-5)

The maximum value of \( g_m \), \( g_{mo} \), will occur at \( V_{GS} = 0 \).

\[
g_{mo} = \frac{2I_{DSS}}{|V_P|}
\] 
(2-6)

From Equation (2-4),

\[
I_D = \frac{g_{mo}}{2} \frac{|V_P|}{2} \left( 1 - \frac{|V_{GS}|}{|V_P|} \right)^2
\] 
(2-7)

When a local oscillator signal \( V_{LO} \sin \omega_{LO} t \) and a signal voltage \( V_{RF} \sin \omega_{RF} t \) along with a bias voltage \( V_{GS} \) are applied between the gate and source terminals, the drain current becomes time varying and is represented by \( i_D \), the total instantaneous drain current. Equation (2-7) becomes:

\[
i_D = \frac{g_{mo}}{2} \frac{|V_P|}{2} \left[ V_P^2 - 2 V_P V_{GS} \right] \left[ \frac{V_{LO}^2}{2} + \frac{V_{RF}^2}{2} \right]
\]  
DC Terms

\[
+ 2 \left( V_{GS} - V_P \right) \left( V_{LO} \sin \omega_{LO} t + V_{RF} \sin \omega_{RF} t \right)
\]  
Fundamental Terms

\[
- \frac{V_{LO}^2}{2} \cos 2\omega_{LO} t - \frac{V_{RF}^2}{2} \cos 2\omega_{RF} t
\]  
2nd Harmonic Terms
\[
\begin{align*}
+ V_{LO} \ V_{RF} \cos(\omega_{LO} - \omega_{RF})t - V_{LO} \ V_{RF} \cos(\omega_{LO} + \omega_{RF})t
\end{align*}
\]

\textit{Sum and Difference Terms}

In general practice, the intermediate frequency is the difference frequency. The term of interest is the intermediate frequency drain current \( i_{\text{DIFF}} \),

\[
i_{\text{DIFF}} = \frac{g_{m0}}{2} \ V_{LO} \ V_{RF} \cos(\omega_{LO} - \omega_{RF})t
\]

\textit{Equation (2-9)}

The conversion transconductance \( g_c \) is defined to be

\[
g_c = \frac{i_{\text{DIFF}}}{V_{RF}} = \frac{g_{m0}}{2} \ \frac{V_{LO}}{V_{P}}
\]

\textit{Equation (2-10)}

Equation (2-10) predicts that FET mixing, because of the square-law characteristics, is independent of gate bias potential, \( V_{GS} \). Experimental investigation, Figure 10 in Chapter 3, indicates that this is not true, because the practical field-effect transistor does not follow the square-law relation perfectly.

The most significant departure from ideal square-law behavior occurs near cutoff. Here the transconductance decreases at a more rapid rate than it does in the remainder of the active region. This departure is believed to be caused by the finite channel dimensions of an FET. The ideal FET model assumes no additional effects at the ends of the channel. Figure 6 shows the departure of \( g_m \) from the ideal conditions. Since an analysis using the square-law relation is not adequate, we must look elsewhere for a method to predict conversion transconductance.
When studying a phenomenon such as mixing one attempts an evaluation based on a single significant parameter. In the analysis of the FET mixer there are two interesting approaches; one based upon the small-signal transconductance $g_m$, and the other concerned with voltage gain $A_v$. Shown in Figures 6 and 7 are plots of transconductance and voltage gain versus static gate voltage for the 2N3823 type FET.

The voltage gain curve was taken at several different values of drain bias to show the effects of internal drain-to-source resistance $r_{ds}$. For values of $V_{DS}$ very much greater than $V_P$ the trend of the voltage gain curve approximates the $g_m$ curve, but this is definitely not the case for small values of drain bias. The $g_m$ data do not include the effects of $r_{ds}$. On the other hand, voltage gain is not an exclusive representation of the device because it depends on an external load.

In the past, several investigators have predicted conversion transconductance in terms of a graph of $g_m$ versus $V_{GS}$. Even though this is not the single significant parameter affecting mixing action, it is advantageous to study both approaches.

The behavior of transconductance $g_m$ versus total instantaneous gate voltage $V_{GS}$ will be represented by the polynomial

$$g_m = a + b\sqrt[3]{V_{GS}} + c V_{GS}^2$$

where $a$, $b$, and $c$ are constants, $b$ and $c$ are normally negative.

Because the local oscillator amplitude is large compared to the RF signal, one can assume that conversion transconductance of an FET

See appendices A and B for the circuit diagram and test procedures.
Fig. 6. Transconductance versus gate voltage for FET type 2N3823.
Fig. 7. Voltage gain versus gate voltage for FET type 2N3823.
at any instant is determined only by the instantaneous amplitude of
the local oscillator, and is independent of the signal voltage. The
gate voltage will then be the sum of the gate bias and local oscil-
lator signal.

\[ |v_{GS}| = |v_{GS}| + v_{LO} \sin \omega_{LO}t \]  \hspace{1cm} (2-12)

Equation (2-11) becomes

\[ g_m = a + b \left( |v_{GS}| + v_{LO} \sin \omega_{LO}t \right) + c \left( |v_{GS}| + v_{LO} \sin \omega_{LO}t \right)^2 \]

or

\[ g_m = a + b |v_{GS}| + b v_{LO} \sin \omega_{LO}t + c |v_{GS}|^2 + 2c |v_{GS}| v_{LO} \sin \omega_{LO}t \]

\[ + c v_{LO}^2 \sin^2 \omega_{LO}t \]  \hspace{1cm} (2-13)

The intermediate frequency (IF) signal is usually the difference
between a higher local oscillator (LO) frequency and a lower signal
frequency (RF). The conversion transconductance \( g_c \) will then result
from the terms of Equation (2-14) which when multiplied by the RF
signal produce the IF signal. That is,

\[ V_{IF} = g_c v_{RF} \sin(\omega_{RF}t) \]  \hspace{1cm} (2-15)

The products necessary to produce the IF are

\[ \left( v_{LO} \sin(\omega_{LO}t) \right) \left( v_{RF} \sin(\omega_{RF}t) \right) = \frac{v_{RF} v_{LO}}{2} \cos(\omega_{LO} - \omega_{RF})t \]

\[ - \frac{v_{RF} v_{LO}}{2} \cos(\omega_{LO} + \omega_{RF})t \]  \hspace{1cm} (2-16)
From Equation (2-14), we obtain

\[ g_c = b V_{LO} \sin \omega_{LO} t + 2c |V_{GS}| \sin \omega_{LO} t \]

\[ = V_{LO} \sin \omega_{LO} t \left( b + 2c |V_{GS}| \right) \]

or

\[ g_c = |V_{LO}| \left( b + 2c |V_{GS}| \right) \]  \hspace{1cm} (2-17)

Equation (2-17) indicates that conversion transconductance is proportional to \( V_{LO} \) and the terms \( b + 2c |V_{GS}| \). For small-signal analysis \( g_m \) depends only on the gate bias \( V_{GS} \), and Equation (2-11) can be represented by

\[ g_m = a + b |V_{GS}| + c |V_{GS}|^2 \]  \hspace{1cm} (2-18)

The slope of Equation (2-13) is

\[ \frac{dg_m}{dV_{GS}} = b + 2c |V_{GS}| \]  \hspace{1cm} (2-19)

Conversion transconductance and therefore conversion voltage gain (the ratio of intermediate frequency voltage at the drain to the RF input signal) is proportional to the slope of the small-signal \( g_m \) versus \( V_{GS} \) curve. This is a very important conclusion, but it is valid only when drain bias is much greater than the pinch-off voltage.

A more accurate analysis would use the voltage gain versus gate voltage curve. This approach is valid for any drain bias, because voltage gain includes the effects of internal drain-source resistance.

The instantaneous output voltage \( V_{ds} \) can be considered related to \( V \) (the sum of RF and LO signal) by the polynomial approximation
\[
\frac{v_{ds}}{v_{gs}} = a + b \left| V_{GS} + v_{gs} \right| + c \left| V_{GS} + v_{gs} \right|^2
\]  
(2-20)

Equation (2-20) can be rearranged to yield

\[
v_{ds} = a' v_{gs} + b' v_{gs}^2 + c' v_{gs}^3
\]

with

\[
a' = a + b \left| V_{GS} \right| + c \left| V_{GS} \right|^2
\]

\[
b' = b + 2c \left| V_{GS} \right|
\]

\[
c' = c
\]  
(2-21)

Mixing is determined by \( b' \) or the slope of the small-signal voltage gain versus gate bias curve. When conditions are such that transconductance and the load resistance completely dictate voltage amplification, \( b \) and \( c \) will have positive values. However, when the internal drain-source resistance \( r_{ds} \) changes appreciably with \( V_{GS} \) (low values of \( V_{DS} \) in Figure 7), \( b \) and \( c \) may take on other signs. It is also possible, as will be discussed later, that a mixing null may result if \( b = -2c \left| V_{GS} \right| \).

In summary of the discussion in this chapter:

1. One would expect conversion voltage gain to be optimum near cutoff.
2. Because of its definition, conversion voltage gain should be independent of RF signal magnitude (Figure 8a).
3. Since conversion transconductance includes the local oscillator voltage, conversion voltage gain should vary directly as the magnitude of the local oscillator signal (Figure 8b).
Fig. 8. Conversion voltage gain versus (a) RF signal strength, (b) LO signal strength.
Several different FET types were used in this study in order to establish an over-all trend rather than relying upon the characteristics of a single transistor type. The transistor types used were:

- 2N3331 p-channel JFET
- 2N3819 n-channel JFET
- 2N3823 n-channel JFET
- 3N125 n-channel JFET
- 2N3796 n-channel MOSFET

Because the 2N3823 FET represents the more technically advanced device of the five, it was used for the majority of the studies. Appendix C contains a summary of the characteristics of the above devices.

Shown in Figure 9 is the circuit diagram used for the study. The signal frequency (RF) and the local oscillator (LO) signal were added arithmetically before application to the gate of the FET. All supply voltages were bypassed to RF through capacitances. A conventional 455 kHz IF transformer (T₁) was used to couple the mixer to a 7.5 megohm load. This load resistance was chosen for maximum IF output. The output was observed on a Tektronix 531 oscilloscope. The LO frequency was set at 1.5 kHz with the RF signal 455 kHz below it at 1.045 MHz. All mixing data were referred to the drain of the transistor in order that the device itself could be evaluated rather than the circuit. The biasing arrangement shown is for an n-channel FET. Gate and drain
Fig. 9. FET mixer circuit diagram.
supply polarities must be reversed for the p-channel device.

The most important single quality measurement of mixing performance is conversion voltage gain, $A_{cg}$. It is defined to be the ratio of RF signal voltage (measured at the gate) to IF voltage output (measured at the drain). To be of value, conversion voltage gain must pertain to a specified local oscillator voltage at the gate.

$$A_{cg} = \frac{V_{IP}}{V_{RF}} \frac{V_{LO \text{ specified}}}{V_{RF}}$$

(3-1)

Relatively small-signal inputs were used (RF = 10 mV, LO = 250 mV) in order to avoid large signal effects.

Experimental evidence presented in Figures 10 through 27 show the effects of changes in a single variable upon conversion voltage gain $A_{cg}$, voltage gain $A_v$, and transconductance $g_m$. All conversion voltage gain data were taken with a local oscillator voltage $V_{LO}$ of 250 mV at 1500 kHz and a signal voltage $V_{RF}$ of 10 mV at 1045 kHz. The voltage gain and transconductance data were taken at 455 kHz.

In general, FET mixing performance with respect to gate bias (Figures 10, 14, 18, 21, and 24) was found to be poor in the square-law region. Conversion voltage gain increased rapidly as cutoff was approached, then fell sharply at cutoff. The rapid fall off of $A_{cg}$ near cutoff can be caused by one of two reasons, depending on the drain bias. Either the instantaneous excursion of the drain can reach into the $BV_{DSS}$ region, or the FET can be driven into cutoff because of the magnitude of the input signals. In the $BV_{DSS}$ region (Figure 1a) the near vertical drain characteristics limit and distort the output. In
all graphs shown, the drain bias was not large enough to cause
operation in the breakdown region. The fall off of $A_{cg}$ was conse-
sequently a simple example of the FET being driven into cutoff by the
inputs ($V_{LO} + V_{RF} + V_{GS}$).

There was very little change in conversion voltage gain with
respect to drain bias (Figures 11, 15, 19, 22, and 25). The response
fell off only when $V_{DS}$ was reduced to below pinch-off.

Included in the figures are graphs of transconductance $g_m$ and
voltage gain $A_v$ versus gate bias. In all cases the optimum conversion
voltage gain occurred in the area where the slope $\frac{\Delta A_v}{\Delta V_{GS}}$ or $\frac{\Delta g_m}{\Delta V_{GS}}$ was
maximum.

The 3N125 FET type with gate $G_2$ tied to the source was the only
transistor that deviated from the trend of best performance near cutoff
(Figure 24). Best mixing, even though poor, occurred at zero gate bias.
Figures 26 and 27, however, show that the largest slopes of $A_v$ and $g_m$
were also at zero gate bias. Therefore all devices performed as was
predicted in Chapter 2.

Since the 3N125 FET has two gates available to control channel
conduction, it seemed conceivable that the transconductance curve could
be shaped, by the potential at the second gate, in order to obtain
optimum mixing performance. This was tried by applying the LO and RF
signals to $G_1$, and a separate bias supply connected to $G_2$. The results
are shown in Figure 23. In each curve the bias at $G_2$ was held constant;
$G_1$ was varied. Using this method, it was possible to change the loca-
tion of maximum mixing, but the conversion voltage gain was poorer than
obtained with $G_1$ and $G_2$ in parallel.
Fig. 10. Conversion voltage gain versus gate voltage for FET type 2N3823.

Fig. 11. Conversion voltage gain versus drain voltage for FET type 2N3823.
Fig. 12. Transconductance versus gate voltage for FET type 2N3823.

Fig. 13. Voltage gain versus gate voltage for FET type 2N3823.
Fig. 14. Conversion voltage gain versus gate voltage for FET type 2N3331.

V\textsubscript{DS} = -15 V

Fig. 15. Conversion voltage gain versus drain voltage for FET type 2N3331.

V\textsubscript{GS} = 4 V
Fig. 16. Transconductance versus gate voltage for FET type 2N3331.

Fig. 17. Voltage gain versus gate voltage for FET type 2N3331.
Fig. 18. Conversion voltage gain versus gate voltage for FET type 2N3819.

Fig. 19. Conversion voltage gain versus drain voltage for FET type 2N3819.
Fig. 20. Transconductance versus gate voltage for FET type 2N3819.
Fig. 21. Conversion voltage gain versus gate voltage for FET type 3N125 (G₁ and G₂ in parallel).

\[ V_{DS} = 20 \, V \]

Fig. 22. Conversion voltage gain versus drain voltage for FET type 3N125 (G₁ and G₂ in parallel).

\[ V_{GS} = -2.2 \, V \]
Fig. 23. Transconductance versus gate voltage for FET type 3N125 (G₁ and G₂ in parallel).
Fig. 24. Conversion voltage gain versus gate voltage for FET type 3N125 (G₂ to source).

Fig. 25. Conversion voltage gain versus drain voltage for FET type 3N125 (G₂ to source).
Fig. 26. Transconductance versus gate voltage for FET type 3N125 (G2 to source).

Fig. 27. Voltage gain versus gate voltage for FET type 3N125 (G2 to source).
Fig. 28. Conversion voltage gain versus gate voltage at various values of $V_{G2S}$ for FET type 2N125.
Thus far all areas of FET nonlinearity have been investigated except the one resulting from forward-biasing the input junction. Since the JFET gate cannot be safely forward biased, a MOSFET was studied. The gate of a MOSFET is insulated from the channel by an oxide dielectric, and can therefore be forward-biased to enhance the channel as well as reversed-biased to deplete it.

The 2N3796 MOSFET used was a rather low gain device with a $g_{mo}$ of $158 \mu$hos and a $V_p$ of 2.4 volts. It is an n-channel depletion type FET requiring a positive potential at the gate to enhance channel conduction. A negative gate potential depletes the channel conduction.

Figure 29 is a graph of conversion gain versus gate voltage for the 2N3796 MOSFET. Both enhancement and depletion modes were investigated. Obviously the enhancement region is a poor choice of operating point for a mixer. Optimum conversion gain was, as with the other devices, near cutoff. As the MOSFET channel conduction was enhanced the transconductance gradually increased and then leveled off to some maximum value. The slope $\frac{\Delta g_m}{\Delta V_{GS}}$ approached zero, resulting in a deterioration of the conversion voltage gain.

Figure 30 is a graph of conversion voltage gain versus drain voltage at the point of optimum gate bias.

When selecting a FET type for mixing service it would be convenient to be able to choose the optimum unit from the manufacturer's specifications and as few measurements as possible. Since the FET's transfer characteristics follow the square-law power relation quite closely, it is obvious from Equation (2-10), rewritten below, that conversion
\[ V_{RF} = 20 \text{ mV AT 1045 kHz} \]
\[ V_{JO} = 250 \text{ mV AT 1500 kHz} \]
\[ V_{DS} = 12 \text{ V} \]

**Fig. 29.** Conversion voltage gain versus gate voltage for MOSFET type 2N3796.

\[ V_{RF} = 20 \text{ mV AT 1045 kHz} \]
\[ V_{JO} = 250 \text{ mV AT 1500 kHz} \]
\[ V_{GS} = -1.7 \text{ V} \]

**Fig. 30.** Conversion voltage gain versus drain voltage for MOSFET type 2N3796.
transconductance is largest from the type with a large $g_{mo}$ and a small $V_P$.

$$g_c = \frac{g_{mo} |V_{LO}|}{2 |V_P|} \tag{3-2}$$

The ratio $\frac{g_{mo}}{|V_P|}$ should be of some importance when selecting the best device. Listed in Table 2 are the measured values of $g_{mo}$ and $|V_P|$ for each unit. The ratio $\frac{g_{mo}}{|V_P|}$ and the maximum conversion voltage gain obtained for each unit are also listed. The device which yielded the largest conversion voltage gain also had the largest ratio of $\frac{g_{mo}}{|V_P|}$.

The units are listed in order of maximum conversion voltage gain, the largest being first. The order of maximum conversion voltage gain $A_{cgm}$ and the ratio $\frac{g_{mo}}{|V_P|}$ are identical. Since best performance was obtained from the device with a large $g_{mo}$ and a small $|V_P|$, a FET can be rated without actually being used in a mixing circuit. Typical values of transconductance can be obtained from the manufacturer.

Pinch-off voltage is usually not available because it may vary widely from unit to unit. The gate bias which reduces the drain current to 0.01 $I_{DSS}$ is a common measurement of $V_P$.

Loci of constant conversion voltage gain are plotted in Figure 31 upon the static drain characteristics of a 2N3823 JFET. The lone point, $A_{cg} = 24$, indicates the largest conversion gain obtainable with the LO signal level used.

The null observed at low drain bias was an area of essentially no mixing. This previously unreported phenomenon, "Conversion Gain Null
TABLE II

<table>
<thead>
<tr>
<th>UNIT</th>
<th>$V_P$</th>
<th>$\varepsilon_{mo}$</th>
<th>$\frac{\varepsilon_{mo}}{V_P}$</th>
<th>$A_{cgm}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>2N3823</td>
<td>2.6</td>
<td>4700</td>
<td>1810</td>
<td>22.5</td>
</tr>
<tr>
<td>2N3819</td>
<td>4.1</td>
<td>5020</td>
<td>1225</td>
<td>19.75</td>
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<td>2N3331</td>
<td>4.2</td>
<td>4000</td>
<td>953</td>
<td>9.5</td>
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<td>2N3796</td>
<td>2.4</td>
<td>1580</td>
<td>654</td>
<td>6.35</td>
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<td>2.42</td>
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<td>6.0</td>
</tr>
<tr>
<td>(G₁ to G₂)</td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3N125</td>
<td>4.46</td>
<td>940</td>
<td>211</td>
<td>2.25</td>
</tr>
</tbody>
</table>

Pertinent characteristics necessary to select the optimum FET type.
Fig. 31. Loci of constant conversion voltage gain superimposed upon common-source drain characteristics.
in FET Mixers, " has been described in the Proceedings of the IEEE; see Appendix D. At the null the third-order component \(c\) of Equation (2-21) was large and opposite in sign to the second order component \(b\) and \(b = -2c V_{GS}\). Figure 32 shows a graph of the third-order term versus gate voltage at a drain-source voltage of 3 volts. Conversion gain is also plotted. The relative magnitude of the third-order term was obtained from a cross-modulation distortion study. The per cent cross-modulation (modulation of the IF by a constant value of undesired modulation carrier) indicates the relative value of the third-order component \(c\). Observe that the third-order component changes phase and becomes large at the gate bias where the mixing null occurred. Analysis using transconductance alone does not predict this null; see Figures 7 and 8.

The theory developed in Chapter 2 predicts that conversion gain is a direct function of the magnitude of the LO signal, and completely independent of the RF signal. This was found to be the case except when the gate bias was such that the device was driven into cutoff, saturation, or some other nonlinear area that limited the output. Figures 33 and 34 are graphs of conversion voltage gain versus RF signal and LO signal respectively. If gate bias is chosen sufficiently distant from saturation or cutoff, such as at \(V_{GS} = 1.5\) volts, the results are as predicted. Deviation from the predicted results occurred only when the LO or RF became very large. It can be seen from the graphs that

---

The theory and method of measurement of cross-modulation are discussed in Chapter 5.
Fig. 32. Cross-modulation (solid line) and conversion voltage gain (broken line) versus gate bias.

2N3823

- $V_{DS} = 20$ V
- $V_{RF} = 10$ mV AT 1045 kHz
- $V_{LO} = 250$ mV AT 1500 kHz

$V_{GS}$ IN Volts
**Fig. 33.** Conversion voltage gain versus RF voltage.

**Fig. 34.** Conversion voltage gain versus LO voltage.
when biased near cutoff the output is limited, and there is no linear relation between the magnitude of the LO and conversion voltage gain, nor is the magnitude of RF independent of conversion voltage gain. Even though there were large-signal limiting effects when biasing was near cutoff, conversion voltage gain is still larger in this area.

From the preceding analysis the following conclusions can be reached concerning the behavior of the FET mixer:

1. Optimum mixing in general occurs at about 80% of pinch-off.
2. The larger the ratio \( \frac{E_{mo}}{|V_{pl}|} \) for any FET, the larger will be the conversion voltage gain.
3. For \( V_{DS} > V_P \), conversion voltage gain was virtually independent of drain bias, \( V_{DS} \).
4. Conversion voltage gain is a direct linear function of LO injection level.
5. Conversion gain is independent of RF injection level.

Other investigators have been engaged in studies similar to that of the author's. Von Recklinghausen reported that conversion gain was approximately proportional to the slope of a plot of \( g_m \) vs. \( V_{DS} \). He also suggested that the local oscillator voltage should not drive the FET into saturation or cutoff. This avoids square wave-modulation of the drain current at the LO frequency. If the LO is too large, the advantages of low spurious responses due to square-law operation are lost, because any device capable of being switched off and on would show the same performance.
Kwok stated that conversion transconductance increases monotonically with LO injection level. For maximum conversion gain the gate should be biased at 0.8 of $V_p$, and the LO signal injected as high as possible.\textsuperscript{7}

To my knowledge no other investigator has concluded that conversion transconductance is optimum for the device with the largest ratio of $\frac{g_{mo}}{|V_p|}$.
CHAPTER 4

CONVERSION NOISE FIGURE

In almost any electronic device, the weakest signal that can be processed is limited by noise that is picked up or generated within it. Because a receiver's low-signal input stages (amplifier and mixer) dictate sensitivity, noise analysis is a very important design consideration.

The term noise figure as applied to an amplifier or a mixer provides a means of specifying the deterioration of the signal-to-noise ratio that results from the noise generated in the transistor and in other circuit components. Since signal-to-noise ratio is the ratio of signal power to noise power at a specified point, the noise factor is the ratio of the input signal-to-noise ratio divided by the output signal-to-noise ratio. This may be written as

$$ F = \frac{S_i/N_i}{S_o/N_o} \quad (4-1) $$

where

- $S_i$ = signal power at the input,
- $N_i$ = noise power at the input,
- $S_o$ = signal power at the output,
- $N_o$ = noise power at the output,
- $F$ = noise factor.

Another widely accepted definition of noise factor is\(^5\)

$$ F = \frac{\text{total available noise power at load}}{\text{available noise power at load due to noise from } V} \quad (4-2) $$
This definition takes into account the thermal noise attributable to the source resistance, $P_C$. If the device contributes no noise, $F$ is unity. Noise figure is usually expressed in decibels.

Equation (4-2) may be written as

$$F = \frac{P_O}{P_i G_a}$$

(4-3)

where $P_O$ is the total available noise power output. This is the power output with no external signal input. The total available noise power input resulting from $P_C$ is $P_i$, and $G_a$ is the available power gain of the stage. The product, $P_i G_a$, is the total noise power at the load due to thermal noise in $P_C$. In specific terms,

$$P_O = \frac{V_O^2}{4 R_O}$$

(4-4)

where $V_O$ is the output noise voltage in the absence of signal voltage, and $P_O$ is the load resistance at the output port. The equation assumes impedance matching. By the same reasoning,

$$P_i = \frac{V_E^2}{4 R_G}$$

(4-5)

where $V_E$ is the equivalent noise voltage at the input due to thermal noise in the input resistance $P_G$, where the thermal noise is produced.

If an external input is now applied to double the available power out ($P_O$), we can write an equation of the form:

$$2P_O = P_O + G_a P_n B_{eq}$$

(4-6)

where $P_n$ is the external power per cycle of bandwidth. The product of
\[ G_a P_n B_{eq} \text{ equals } P_o. \] Also

\[ P_n = \frac{V_{ng}^2}{4 P_C} \]  \hspace{1cm} (4-7)

where \( V_{ng} \) is the external noise voltage necessary to double the available power out.

From Equation (4-6),

\[ G_a = \frac{P_o}{P_n B_{eq}} \]  \hspace{1cm} (4-8)

Equations (4-3) and (4-8) may be combined to form

\[ F = \frac{P_n B_{eq}}{P_i} \]  \hspace{1cm} (4-9)

Then from Equations (4-5) and (4-7), Equation (4-9) becomes

\[ F = \frac{V_{ng}^2 B_{eq}}{V_g^2} \]  \hspace{1cm} (4-10)

Since \( V_g \) is thermal noise, it may be written as

\[ V_g^2 = 4kT B_{eq} P_C \]  \hspace{1cm} (4-11)

where \( k \) is Boltzmann's constant,

\( T \) is temperature in degrees Kelvin,

\( P_C \) is the input source resistance,

\( B_{eq} \) is the bandwidth.

Then, from Equation (4-10), it follows that

\[ F = \frac{V_{ng}^2}{4kT P_C} \]  \hspace{1cm} (4-12)
Equation (4-12) is the basic noise factor equation; but it can, under certain methods of noise measurement, take another form. There are two test methods commonly used for noise measurements. They are called the noise-generator method and the single-frequency signal-generator method.

The noise-generator method consists of comparing the noise actually present \( (P_o) \) with the noise produced by a noise-signal generator. This method has the advantage that no measurements need be taken on the amplifier or mixer. Only the noise power necessary to double the available output power is required. When this method is used, Equation (4-12) is the correct noise factor relation.

When using the single-frequency method, the noise generator is replaced by a sine-wave signal generator. This method is more accurate when dealing with large values of noise figure, as in a mixer. Since the input is a discrete frequency the noise factor equation takes the form

\[
F = \frac{V_s^2}{4kT B_{eq} R_G}
\]

(4-13)

The single-frequency signal-generator method was chosen for this study.

In the noise factor equation, Equation (4-13), the source resistance \( R_G \) is the Thévenin equivalent looking back from the gate of the FET into the input circuit; \( V_{ng} \) or \( V_s \) is the open-circuit voltage of the input circuit with the gate open.

Because noise consists of random transients, a definition for bandwidth other than that used for a standard tuned circuit must be employed for noise calculations. Where noise is concerned, our interest is not
in the amplitude of the response, but in the area under the frequency response curve which corresponds to noise power. The bandwidth used in noise calculations is the bandwidth of an ideal bandpass circuit that has a rectangular response of the same area and peak value \( P_m \) as the actual amplifier circuit (Figure 35). \(^9\)

\[
P_m = 2 P_{eq}
\]

\[
\int_0^{\infty} P(f) \, df = 2 P_{eq}
\]

If the curve represents the noise voltage \( V_n \) as a function of frequency, Equation (4-14) becomes

\[
\int_0^{\infty} V_n^2(f) \, df = \pi P_{eq}
\]

**Fig. 35.** Practical response curve and equivalent rectangular response of a tuned circuit.
where \( v_m \) is the maximum value of the actual response. Then, from Equation (4-15), we obtain

\[
B_{eq} = \frac{\int_{0}^{\infty} v^2 (f) df}{v_m^2}
\]

(4-16)

If the same circuit is used as an amplifier and as a mixer, a relationship may be derived to correlate the noise factors. When operating as an amplifier, the input frequency will be simply the intermediate frequency. As a mixer, the difference \((\omega - \omega_{RF})\) is the intermediate frequency.

As an amplifier, the noise factor \( F_a \) is

\[
F_a = \frac{V_{sa}^2}{4kT B_{eq}}
\]

(4-17)

where \((V_{sa})^2\) is the mean square input voltage necessary to double the available noise power out \( P_o \).

As a mixer the conversion noise factor \((F_c)\) is

\[
F_c = \frac{V_{sc}^2}{4kT B_{eq}}
\]

(4-18)

where \((V_{sc})^2\) is the mean square RF input voltage to double the available noise power out \( P_o \). The local oscillator voltage is held constant.

Since the same circuit is used in each type of measurement, the source resistance and the equivalent bandwidth are identical. The ratio of the conversion noise factor to amplifier noise factor is

\[
\frac{F_c}{F_a} = \frac{V_{sc}^2}{V_{sa}^2} \left( \frac{kT B_{eq} R_o}{kT B_{eq} R_o} \right)
\]

(4-19)
or
\[
\frac{F_c}{F_a} = \frac{V_{sc}^2}{V_{sa}^2}
\]  
(4-20)

Recall that the equation for voltage gain \(A_v\) is
\[
A_v = g_m R_{sh}
\]  
(4-21)

where \(g_m\) is the transconductance, and \(R_{sh}\) is the load resistance.

Therefore
\[
V_{sa}^2 = \left( \frac{V_x}{g_{ma} R_{sh}} \right)^2
\]  
(4-22)

where \(V_x\) is the output voltage with output power doubled,
\(g_{ma}\) is the transconductance of the FET (the \(a\) indicates operation as an amplifier),
\(R_{sh}\) is the load resistance including internal drain source resistance and load resistance.

Also
\[
V_{sc}^2 = \left( \frac{V_x}{g_{mc} R_{sh}} \right)^2
\]  
(4-23)

where \(g_{mc}\) is the conversion transconductance of the FET. Since the same circuit is used for both types of operation, the available noise power output \(P_o\) is the same in each case. This means that \(V_x\) and \(R_{sh}\) for the last two equations are equivalent. When the relations for \(V_{sa}\) and \(V_{sc}\) are substituted into Equation (4-20), the ratio of the noise factors becomes equal to the square of the inverse transconductance ratio
\[
\frac{F_c}{F_a} = \left( \frac{g_{ma}}{g_{mc}} \right)^2
\]  
(4-24)
The above relation may be simplified still more because

\[ A_v^2 = \left( \frac{g_{mA}}{R_{sh}} \right)^2 \]  

(4-25)

or

\[ g_{ma}^2 = \left( \frac{A_v}{R_{sh}} \right)^2 \]  

(4-26)

Likewise

\[ A_{cg}^2 = \left( \frac{g_{mc}}{R_{sh}} \right)^2 \]  

(4-27)

or

\[ g_{mc}^2 = \left( \frac{A_{cg}}{R_{sh}} \right)^2 \]  

(4-28)

The noise factor ratio then becomes

\[ \frac{F_c}{F_a} = \left( \frac{A_v}{A_{cg}} \right)^2 \]  

(4-29)

If conversion voltage gain, voltage gain, and amplifier noise factor are known, the conversion noise factor can be determined. This relation means that the operation of a mixer can be predicted from noise measurements on the device operated as an amplifier.

The circuit diagram and test procedures for the noise analysis are contained in Appendix E.

Shown in Figures 36 and 37 are experimental curves of amplifier noise factor and conversion noise factor versus gate and drain bias potential. As an amplifier, the noise factor reached a minimum of 5.5 db at \( V_{GS} = 0 \), and gradually increased as \( V_{GS} \) was increased. The lowest noise was in the area of high voltage gain.
Fig. 36. Conversion and amplifier noise factor versus gate voltage.

Fig. 37. Conversion and amplifier noise factor versus drain voltage.
As a mixer the conversion noise factor was lower in the area of high conversion voltage gain, near cutoff. The noise factor was considerably higher in the square-law region where mixing performance was found to be poor.

The drain voltage (Figure 37) does not have a marked effect on noise factor. This was expected, since voltage gain and conversion voltage gain do not change a great deal with drain bias.

Figures 38 and 39 are curves of conversion gain and voltage gain versus gate voltage. From this information and from the amplifier noise factor curve (Figure 36), the conversion noise factor was calculated using the relation

\[ F_c = F_a \left( \frac{A_v}{A_{cc}} \right)^2 \]  

(4-30)

The predicted conversion noise factor is shown on Figure 36. All data for this curve were taken at the same drain potential. The experimental and predicted conversion noise factor curves do not differ by more than 1 db at any point.

The noise factors obtained in this study were somewhat higher than that of other investigators, but the indicated trends are correct. Kuok stated that minimum noise factor was obtained where \( g_c \) was maximized. Therefore conversion gain and conversion noise factor are optimum at the same gate bias. Kuok obtained conversion noise factor values from 6 db up for a different FET type. Typical FET amplifier noise factors range from 2 to 4 db. The main difficulty arose from having to depend on the accuracy of the spectrum analyzer to measure the magnitude of very small signals.
Fig. 38. Conversion voltage gain versus gate voltage for FET type 2N3823.

Fig. 39. Conversion voltage gain versus drain voltage for FET type 2N3823.
CHAPTER 5

CROSS-MODULATION DISTORTION

As previously noted, mixing results from a nonlinear curvature of the gate-to-drain transfer characteristics. Second and third-order nonlinearities of the transfer characteristics are the principal contributors to mixing action. Normally, spectral components differing from the intermediate frequency are of little concern, because they can be eliminated easily by frequency selective networks in the output circuit. There are, however, properties of the FET characteristics which will yield frequency components that are either a part of the IF signal, or that fall within the bandpass of the output circuit. Knowledge of these distortion components plays an important role in mixer design.

Numerous extraneous frequencies are normally present in the front end of a receiver. These frequencies may mix with each other and with the local oscillator to generate spurious frequency components at or near the intermediate frequency. The term used to describe this action is intermodulation distortion. Intermodulation distortion is mainly the result of third-order nonlinearities of the transfer characteristics.

Another type of third-order distortion, known as cross-modulation, has the effect of transferring modulation from the undesired signal to the intermediate frequency signal. Cross-modulation cannot be eliminated by tuned circuits in the output of the mixer. An example of cross-modulation is illustrated in the following discussion. The receiver is tuned to a desired signal. At the same time, a strong
"unwanted" signal at a frequency not greatly different from that of the desired is simultaneously present. During the intervals when the carrier wave of the desired station is unmodulated, the modulation of the unwanted signal is heard, but if the desired signal is turned off, the interference from the unwanted signal disappears.\(^\text{16}\)

Cross-modulation is rather hard to visualize, but it can be shown to exist mathematically. Consider the instantaneous output voltage \(v_{ds}\) to be related to the input voltage \(v_{gs}\) by the polynomial approximation,

\[
v_{ds} = a' v_{gs} + b' v_{gs}^2 + c' v_{gs}^3
\]

where, \(a'\) is the small-signal gain,

\[
a' \approx g_m R_L
\]

\(b'\) is the conversion gain,

\[
b' \approx g_c R_L
\]

where

\[
g_c \approx \frac{d g_m}{d v_{gs}} \quad \text{(the conversion transconductance)}
\]

and \(c'\) is

\[
c' \approx g_c' R_L
\]

where

\[
g_c' = \frac{d g_c}{d v_{gs}}
\]

The input voltage consists of the sum of the RF and an undesired signal, \(v_u\).
\[ v_{gs} = V_{RF} \sin \omega_{RF} + V_U \sin \omega_U^t \]  

(5-7)

The cubing of the input \( v_{gs}^3 \) will yield

\[
v_{gs}^3 = \left( \frac{3}{4} V_{RF} + \frac{3}{2} V_{RF} V_U^3 \right) \sin \omega_{RF}^t + \left( \frac{3}{4} V_U^3 + \frac{3}{2} V_{RF} V_U \right) \sin \omega_U^t - \frac{V_{RF}^3}{4} \sin 3\omega_{RF}^t - \frac{V_U}{4} \sin 3\omega_U^t
\]

\[- \frac{3}{4} V_{RF}^2 V_U \sin \left( \frac{2\omega_{RF} + \omega_U}{4} \right)^t - \frac{3}{4} V_{RF}^2 V_U \sin \left( -2\omega_{RF} + \omega_U \right)^t
\]

\[- \frac{3}{4} V_{RF} V_U^2 \sin \left( \omega_{RF} + 2\omega_U \right)^t - \frac{3}{4} V_{RF} V_U^2 \sin \left( \omega_{RF} - 2\omega_U \right)^t
\]

(5-8)

In Equation (5-8), the term of particular importance is \( \frac{3}{2} V_{RF} V_U^2 \), because the output obtained at frequency \( \omega_{RF} \) is dependent to some extent upon the amplitude of the signal component of frequency \( \omega_U \). This effect is cross-modulation, since it causes the amplitude of an amplified signal of one frequency to be dependent upon the amplitude of a signal component having a different frequency. It will be shown that cross-modulation is also present on the IF carrier.

From Equation (5-8), the third-order term in Equation (5-1) contains the term

\[ c' \left( \frac{3}{2} V_U^2 V_{RF} \sin \omega_{RF}^t \right) \]

(5-9)

Since the local oscillator signal is very much larger than the RF signal, we may assume that conversion transconductance is determined only by the instantaneous amplitude of the local oscillator, and is independent of the signal voltage. \(^{15}\) Because the LO is a sinusoidal
signal and a function of $g_c$, $g'_c$ will also be a function of the LO signal. We can therefore rewrite that

$$g'_c = k \sin(\omega_{LO} t)$$  \hspace{1cm} (5-10)

where $k$ is a constant. Then, from Equation (5-9), the output $v_{ds}$ contains

$$\frac{3}{4} \frac{V_{RF}}{V_U} \frac{V_U^2}{k R_L} \sin(\omega_{LO} t) \sin(\omega_{RF} t)$$  \hspace{1cm} (5-11)

Therefore, the cross-modulation component on the IF carrier is

$$\frac{3}{4} \frac{V_{RF}}{V_U} \frac{V_U^2}{k R_L} \cos(\omega_{LO} - \omega_{RF}) t$$  \hspace{1cm} (5-12)

The undesired signal is amplitude modulated, so it has the form

$$V_U = V \left( 1 + m \sin(\omega_a t) \right)$$  \hspace{1cm} (5-13)

The cross-modulation component is

$$k' \left( 1 + m^2 \sin^2(\omega_a t) + 2m \sin(\omega_a t) \right) \sin(\omega_{IP} t)$$  \hspace{1cm} (5-14)

where

$$k' = \frac{3}{4} \frac{V_{RF}}{V_U} \frac{V_U^2}{k R_L}$$  \hspace{1cm} (5-15)

Thus one concludes that modulation from the undesired signal is transferred to the IF carrier.

At present there is confusion concerning the method of measurement of cross-modulation. There seems to be no set specification for cross-modulation rejection in a mixer. The method normally adopted for the measurement of cross-modulation consists of increasing the magnitude of the undesired signal with a constant per cent modulation until a
specified per cent of cross-modulation is observed on the unmodulated intermediate frequency carrier. For proper operation, it is desired to have better than -20 db cross-modulation for a 13 mV interfering signal.\textsuperscript{18}

The criterion used to evaluate the FET mixer is as follows. The RF and LO signals were held constant; both were unmodulated. The undesired signal, 30\% modulated at 400 Hz, was increased in amplitude until 3\% cross-modulation appeared on the IF output of the mixer. The undesired signal level was then recorded. Experiment shows that cross-modulation depends only on the level of the undesired signal, and not on the RF signal.\textsuperscript{18} The frequency of the undesired signal was not critical since the input to the FET mixer was not a tuned circuit. The only requirement of the undesired signal frequency was that it must not cause intermodulation components.

Figure 40 shows a block diagram of the FET mixer cross-modulation test circuit. Circuit diagram and test procedures used are given in Appendix F.

\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{fig40.png}
\caption{Block diagram of cross-modulation test circuit.}
\end{figure}
The representations in Figures 41 through 44 depict the results of the cross-modulation distortion test. The figures include graphs of the magnitude of undesired (30% modulated at 400 Hz) to yield 3% cross-modulation versus gate bias voltage (with $V_{DS} > V_P$), and undesired versus drain bias with constant gate bias. Figure 32 in Chapter 3 was a direct measurement of the third-order term since the amount of cross-modulation was measured rather than the level of the undesired. For the following figures, a large undesired signal indicates very little third-order component present; a small undesired signal indicates a large amount of third-order distortion.

The data for Figure 41 was taken at three different levels of RF signal. This substantiates the fact that cross-modulation depends only on the level of the interfering signal. The graphs indicate that cross-modulation (third-order component of the transfer characteristics) was greatest near saturation and cut-off. In the area of $V_P/2$, an undesired signal as large as 900 mV was required to obtain the specified amount of cross-modulation. This indicates very little third-order curvature present.

The only area that might cause cross-modulation distortion of any consequence was near cutoff, where gate bias approached pinch-off. This was also the area of optimum conversion voltage gain. The worst condition obtained for cross-modulation distortion was a 30 mV undesired signal for the 2N3823 FET. Comparing this with the 13 mV minimum specification given earlier indicates that there is very little third-order behavior present in the FET characteristics.
The two sharp peaks in Figure 42 indicate a phase shift (change of sign) in the third-order component.

As seen by Figure 44 cross-modulation distortion does not depend a great deal on drain bias potential.

Kwok reports in his investigation of the FET as a mixer that cross-modulation was minimum when the device was operated in the square-law region. Also, high injection of the LO improved cross-modulation performance. Kwok measured the undesired signal necessary to produce 1% cross-modulation, and obtained results comparable to those given here.7
V_{RF} AT 1045 kHz
V_{LO} = 250 mV AT 1500 kHz
V_{U}: 30\% MOD., 400 kHz AT 880 kHz
V_{DS} = -15 V

---

**Fig. 41.** Undesired signal to produce 3\% cross-modulation versus gate voltage for FET type 2N3331.
Fig. 42. Undesired signal to produce 3% cross-modulation versus gate voltage for FET type 2N382A.
Fig. 43. Undesired signal to produce 3% cross-modulation versus gate voltage for FET type 34125 (G2 and G1 in parallel).
$V_{RF} = 20 \text{ mV AT 1045 kHz}$
$V_{LO} = 250 \text{ mV AT 1500 kHz}$
$V_U; 30\% \text{ MOD.}, 400 \text{ Hz AT 880 kHz}$
$V_{GS} = 4 \text{ V}$

Fig. 44. Undesired signal to produce 75% cross-modulation versus drain voltage for FET type 2N3331.
CHAPTER 6

HIGH FREQUENCY MIXING

All of the topics thus far discussed have dealt with the field-effect transistor as a low-frequency mixer. This chapter describes studies of the FET operated as a mixer at frequencies up to 125 mHz. The intermediate frequency was maintained at 455 kHz.

High-frequency operation of the FET is best examined by evaluating the frequency dependence of the common-source admittance parameters. For a typical FET type (2N3823) the input admittance remains susceptive up to about 200 mHz, and the reverse transfer admittance is dominated by the feedback capacitance from drain-to-gate. The forward transfer admittance is essentially constant and real up to 60 mHz. Beyond 60 mHz, the magnitude of the forward transfer admittance begins to decline, and real and imaginary components become equal at about 300 mHz. The output admittance remains predominately capacitive at all frequencies.

In Figure 5 the common-source FET model was approximated by capacitive elements from gate-to-drain, gate-to-source, and drain-to-source. At low frequencies the capacitances have little effect on operation and usually may be omitted from consideration. At higher frequencies the drain-to-source capacitance becomes a low impedance in shunt with the output, and the gate-to-drain capacitance provides a low impedance path to the input signal. The ultimate effect is unity voltage gain when the gate-to-drain capacitance appears as a short.
Because of the above mentioned considerations, one can expect the voltage-gain bandwidth of a simple uncompensated FET amplifier to be quite small. A type 2N3823 FET with a 5000 ohm resistive load was studied and found to have a bandwidth of about 8 mHz. The bandwidth was measured experimentally and determined analytically. Analysis was made by using measured component values in the equivalent circuit. Results of both approaches were in agreement.

Behavior of a FET mixer is, naturally, different from that of an amplifier. The load on a mixer is a tuned circuit resonant only at the intermediate frequency. Other frequency components present at the load will see a short circuit. The conditions at the load are independent of the LO and RF frequencies, and the gate-to-drain and drain-to-source capacitances do not limit the bandwidth.

The only parameters significantly affecting high-frequency operation are the reduction in input impedance because of the input capacitance, and the decrease in small-signal transconductance.

Conversion transconductance for a fixed local oscillator voltage was found to be proportional to the slope of the small-signal transconductance versus gate-bias voltage curve. The bandwidth of a mixer results from reduction in the slope of $\frac{\Delta A_{g}}{V_{GS}}$ with frequency. Since cutoff $(V_{GS} = V_{P})$ is a static condition independent of frequency, deterioration of the transconductance slope can be determined by measuring $g_{m0}$ ($g_{m}$ at $V_{GS} = 0$) at various frequencies. When transconductance becomes complex, $\left| g_{m} \right|$ must be measured.
The transconductance of a 2N3823 FET was measured at 1 mHz and at 100 mHz. The value at 100 mHz was about 10 per cent lower than the 1 mHz value. This indicates that conversion voltage gain will deteriorate quite slowly with increased frequency while voltage gain will fall off rather rapidly.

Shown in Figure 45 is an experimental plot of conversion voltage gain versus frequency. Input measurements were taken at the gate to eliminate the effect of input capacitance. Note that the mixing response fell off very gradually with frequency. The bandwidth was near 100 mHz.

In general, frequency did not influence the shape of the curve of conversion gain versus gate-bias voltage. Only a gradual decrease in magnitude was noted. This is illustrated by Figure 46 which is a graph of conversion voltage gain versus gate bias voltage for an RF signal of 1, 75, and 125 mHz. Conversion voltage gain fell off most rapidly at low bias voltages. This indicates a somewhat smaller change in the slope \[ \frac{4g_m}{\Delta V_{GS}} \] near cutoff than at saturation. This is possible since the FET transfer characteristics deviate somewhat from the square-law approximation at cutoff.

There obviously is not a direct correspondence between the deterioration of the transconductance slope and the bandwidth of conversion voltage gain, but it appears that transconductance is the most important parameter affecting high-frequency operation of the FET mixer.

* A General Radio Company type 1607-A Transfer-function and Impedance Bridge was used for the high-frequency measurement.
Fig. 45. Conversion voltage gain versus signal frequency.
2N3823
$V_{DS} = 20$ V
IF AT 455 kHz
$V_{RF} = 10$ mV
$V_{IO} = 250$ mV

**Fig. 46.** Conversion voltage gain versus gate voltage at several values of signal frequency.
CHAPTER 7

CONCLUSIONS

The objective of this dissertation has been to evaluate the important design considerations of the FET mixer. The topics covered were optimum biasing potentials, considerations for selecting the optimum FET type, conversion noise factor, cross-modulation distortion, and high frequency mixing. The following is a summary of important conclusions.

OPTIMUM BIASING: Conversion transconductance was described as being proportional to the slope of a plot of either transconductance or voltage gain versus gate bias voltage. The validity of the two descriptions depended on the drain bias. The voltage gain approach was valid for all $V_{DS} > V_p$. In general, optimum mixing occurred in the cutoff area (where the slope was the largest) with $V_{GS}$ about 80% of $V_p$. Transconductance approached zero in the cutoff region much faster than the square-law approximation predicted. This deviation resulted in optimum conversion voltage gain. The enhancement region of a MOSFET was also investigated, but conversion voltage gain was found to be quite low.

Maximum conversion gain resulted from the unit with the largest value of $g_{mo}$ and the smallest value of $V_p$. This combination is important in selecting a FET type.

Conversion voltage gain was found to be independent of drain bias for $V_{DS} > V_p$. The response fell off only when $V_{DS}$ was reduced below
pinch-off. Biasing of \( V_{DS} \) below \( V_P \) should also be avoided because of the mixing null observed.

The dual-gate FET performed best when the gates were connected in parallel. This arrangement yielded the maximum transconductance and lowest \( V_P \) obtainable.

As expected, the conversion gain varied directly with the magnitude of the LO; and it was independent of the magnitude of the RF signal.

CONVERSION NOISE FACTOR: The relationship

\[
F_c = F_a \left( \frac{A_v}{A_{cc}} \right)^2
\]

(7-1)

was developed to predict conversion noise factor \( F_c \) from a knowledge of amplifier noise factor \( F_a \), voltage gain \( A_v \), and conversion voltage gain \( A_{cc} \). The predicted conversion noise factor was compared with experimental data and found to be in good agreement.

Conversion noise factor was lowest near cutoff where conversion gain was optimum. Highest values were observed near saturation. Drain bias again had little effect on conversion noise factor.

CROSS-MODULATION DISTORTION: For proper mixing operation it is desirable to have better than -20 dB cross-modulation for a 13 mV interfering signal. This specification was achieved for all devices tested at all operating points.

Cross-modulation distortion was found largest near cutoff. This was unfortunate but still within the specifications. The distortion was almost nonexistent at other gate biasing points.
HIGH FREQUENCY MIXING: Transconductance was found to be the important parameter influencing mixing at high frequencies. The bandwidth of the mixer was limited primarily by the deterioration in $\frac{\Delta g_m}{\Delta V_{GS}}$ with increasing frequency. Since cutoff is a static condition independent of frequency, the deterioration of the transconductance slope was determined by measuring $|V_{fs}|$ at various frequencies. The bandwidth of the 2N3823 type FET mixer was about 100 mHz. Optimum performance at high frequency was still near cutoff.
## REFERENCES


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21. Wollesen, Donald L., Understanding Field-effect Transistor Parameters, Motorola Application Note AN-205.

APPENDICES
APPENDIX A

MEASUREMENT OF VOLTAGE GAIN

Shown in Figure 47 is the circuit diagram used to evaluate the FET as a simple voltage amplifier. With the exception of the input, the circuit was essentially the same as the mixer test circuit (see Chapter 3). A single input at the intermediate frequency was used. A conventional 455 kHz IF transformer (T₁) was used to couple the mixer to a 7.5 megohm load. This load resistance was chosen for maximum output. The biasing arrangement shown is for an n-channel FET. Gate and drain supply polarities must be reversed for the p-channel device. Voltage gain $A_v$ is given by

$$A_v = \frac{V_o}{V_i}$$

Fig. 47. Voltage gain test circuit.
APPENDIX B

MEASUREMENT OF TRANSCONDUCTANCE

Small-signal transconductance was measured by using the circuit shown in Figure 48. The circuit will accommodate both n-channel and p-channel devices. Physical construction limited operation of the circuit to frequencies below 2 mHz.

Voltage gain of a FET stage at low frequencies was approximated by

\[ |A_v| = \varepsilon_m R_L \]

This relation becomes accurate if employed where the output resistance of the FET is large enough to be neglected and the input impedance is infinite. The 100-ohm load used in the drain circuit permits the output resistance to be disregarded because \( r_{ds} \) is always very much larger than 100 ohms. At low frequencies the input impedance is essentially infinite. Small-signal transconductance is determined by

\[ \varepsilon_m = \frac{V_o}{(100) V_1} \] (\( \mu \) mhos)
Fig. 48. Small-signal transconductance test circuit.
## APPENDIX C

### SUMMARY OF MANUFACTURERS' LITERATURE ON FET TYPES USED

<table>
<thead>
<tr>
<th>Device</th>
<th>Parameter and test conditions</th>
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</tr>
</thead>
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<tr>
<td></td>
<td><strong>$V_{DS}$</strong></td>
<td><strong>$V_{GS(OFF)}$</strong></td>
</tr>
<tr>
<td></td>
<td><strong>(mA)</strong></td>
<td><strong>(Volts)</strong></td>
</tr>
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<td>2N3331</td>
<td>0.5 -15</td>
<td>-10 V</td>
</tr>
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<td>$V_{GS} = 0$</td>
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<td>15 V</td>
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<td>$V_{GS} = 0$</td>
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<td>$V_{GS} = 0$</td>
</tr>
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</table>
Conversion Gain Null in FET Mixers

Abstract—Minima of conversion gain are observed in FET mixers at rather low levels of drain-source voltage. This phenomenon is described by contours of constant conversion gain on the static drain characteristics. The explanation given in terms of polynomial coefficients is substantiated by cross-modulation data.

In the course of studying the signal mixing capabilities of the junction field-effect transistor, one is concerned by minima of conversion gain exhibited by the mixing circuit when the device is operated at relatively low levels of drain-source voltage. Normal engineering practice would preclude operation in the vicinity of any such region of inefficient behavior; however, investigation of this phenomenon provides a better understanding of the device and the mixing process.

Locii of constant conversion gain are sketched in Fig. 1 upon the static drain characteristics of a 2N3823 N-channel FET. The trends shown in this experimentally-derived data are not limited to the transistor type mentioned. The RF was 10 mV at 1020 kHz, with local oscillator of 250 mV at 1500 kHz. The stage load was a conventional IF tank tuned to 480 kHz. An explanation for the locus of minimum conversion gain will be discussed and experimental verification offered.

In a typical FET mixer the modulated signal and the local oscillator wave are added arithmetically before application to the gate of the FET; their sum will be symbolized by \( v_{gs} \). Conversion to an IF is accomplished by virtue of the nonlinear relationship between drain current and gate voltage, as discussed in the literature.\(^1\) The instantaneous output voltage \( v_o \) will be considered to be related to \( v_{gs} \) by the polynomial approximation,

\[
\frac{v_o}{v_{gs}} = a + b|V_{GS} + v_{gs}| + c|V_{GS} + v_{gs}|^2
\]

with \( V_{GS} \) representing the dc gate-source bias voltage. Equation (1) can be rearranged to yield

\[
v_{gs} = a'v_{gs} + b'v_{gs}^2 + c'v_{gs}^3
\]

with

\[
a' = a + b|V_{GS}| + c|V_{GS}|^2
b' = b + 2c|V_{GS}|
c' = c.
\]

The quantity \( a' \) represents the small-signal voltage gain of an amplifying stage. For stages wherein the transconductance \( g_m \) and the load resistance completely dictate voltage amplification, \( b \) and \( c \) will have positive values.
But in many practical cases the internal drain-source resistance $r_{ds}$ changes appreciably with $V_{GS}$. Under such circumstances voltage amplification may reach a peak before eventually declining at large values of $V_{GS}$ because of the normal reduction in $g_{m}$.

Conversion gain, the ratio of intermediate frequency voltage at the drain to the modulated signal input is determined from (2) to be

$$A_{CG} = b' V_{0m}$$  \hspace{1cm} (3)

with $V_{0m}$ the peak value of the local oscillator wave. As we have seen, $b'$ is dependent upon coefficients $b$ and $c$ of (1). At certain low gate-source bias levels and low values of $V_{GS}$, $c$ is observed to be a negative quantity, its sign reverting to positive at higher gate voltages. Mixing, determined by $b'$, may be reduced to zero under the condition that $b = -2c|V_{GS}|$. It is to be expected that this mixing null will be experienced at the point where the magnitude of $c$ is maximized, since $b$ is determined primarily by the behavior of $g_{ms}$, and thus represents a general decline in gain as $V_{GS}$ increases in value.

Cross-modulation distortion is determined directly by the coefficient of the third-order term, $c$. The representation in Fig. 2 depicts percent cross modulation (modulation of IF by a constant value of undesired modulated carrier) versus gate bias voltage at a drain-source potential of 3 volts. The data apply for a 100-mV, 840 kHz undesired signal introduced at the gate.
30 percent modulated by 400 Hz. Conversion gain is also plotted. The phase change apparent in the cross-modulation curve represents a sign change in the coefficient $c$. For values of cross modulation below the zero level, the $c$ term effectively subtracts from the predominant mixing term $b$, causing a reduction in conversion gain that, under certain circumstances, can approach a value of zero.

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APPENDIX F

MEASUREMENT OF NOISE FACTOR

Shown in Figure 49 is the circuit diagram used for the noise factor analysis. Both amplifier and conversion noise factors were determined by the use of this circuit. As an amplifier the circuit functioned with one input at the center (IF) frequency. As a mixer the difference frequency \((\omega_{\text{LO}} - \omega_{\text{RF}})\) equaled the center frequency. Because we are dealing with random noise, it was necessary to measure the output with a voltmeter which responded to the rms value of its input signal for all waveforms.

Before taking measurements it was first necessary to determine the Thevenin equivalent resistance \(R_G\) and the equivalent bandwidth of the circuit \(B_{\text{eq}}\), see Equation (4-13). Noise measurements were then taken using the Single-frequency Signal-generator Method of evaluating noise factor.\(^{16}\)

The circuitry to the left of line \((1,1')\) indicates the input circuit. The Thevenin equivalent resistance of this is represented by \(R_G\). The Thevenin equivalent was found as follows: with terminals \((1,1')\) open, an \(rf\) signal was applied at the center frequency \((350 \text{ kHz})\). A resistance was then inserted across \((1,1')\) such that the above voltage was halved. This value of resistance is the source resistance \(R_G\). Its value was not affected by the value of \(P\) (Figure 49). Since the \(I_0\) was in shunt at the input, the equivalent resistance was essentially equal to the output resistance of the signal generator \((50 \text{ ohms})\). Note that
Amplifier - Hewlett-Packard Model 465A Amplifier.
Voltmeter - Hewlett-Packard Model 3400A RMS Voltmeter.
T<sub>1</sub>, T<sub>2</sub> - Conventional 455 kHz IF transformers detuned to 350 kHz because of amplifier input.
R - 180 K when operated as an amplifier, 34 K as a mixer.

Fig. 49. Noise factor analysis test circuit.
the LO generator must be left in the circuit for both amplifier and mixer measurements.

The equivalent bandwidth $B_{eq}$ needed for the noise analysis was found by applying noise from a General Radio type 1390-B Random Noise Generator, and observing the output response on a Singer SPA-3/25a Spectrum Analyzer. The result was plotted to yield an amplitude as a function of frequency curve (Figure 50). The data amplitude points were then squared point by point to yield a graph of amplitude response squared as a function of frequency (Figure 51). By a method of counting squares, the integral in Equation (4-16) was approximated. The bandwidth was found to be 16.4 kHz.

**Single-frequency Signal-generator Method of Evaluating Noise Factor.**

As an Amplifier: With the signal generator producing no signal (i.e. with $V_s = 0$), but with the input circuit $R_G$ in place, the noise power output was observed. This corresponds to the noise power output under normal conditions of operation, taking into account the thermal noise of $R_G$ and the imperfections of the system. The signal generator was then turned on and its available power adjusted until the observed noise output power was twice the noise power corresponding to the noise power when the signal generator was inactive. In other words, the signal generator was adjusted until the observed voltage was increased by $\sqrt{2}$ thereby doubling the noise power output. Since $k$ (Boltzmann's constant), $T$ (temperature in degrees Kelvin), $R_G$ (input resistance), $F_{eq}$ (bandwidth), and now $V_s$ (signal voltage to double the
Fig. 50. Noise voltage response versus frequency.

Fig. 51. Noise voltage response squared versus frequency.
noise power) are all known, the amplifier noise factor can be determined directly from Equation (4-13), repeated below.

\[ F_a = \frac{V_s^2}{4kT_B eqR_G} \]

As a Mixer: The procedure for determining conversion noise factor was the same as for the amplifier except that two inputs were used (RF and LO). The difference frequency equaled the center frequency used for the amplifier noise test. The LO was held constant and the RF was increased to double the available output power.

Since \( V_s \) is the voltage at the gate of the FET, it was necessary to know the ratio of the input voltage to the gate voltage. This ratio was determined with the aid of the spectrum analyzer, and found to be extremely small. Consequently, one deals with very small signal levels when measuring noise. This can be difficult if equipment is not accurate.
APPENDIX F

CROSS-MODULATION TEST PROCEDURES

Figure 52 contains the circuit diagram of the mixer test circuit used for the cross-modulation study. This circuit was basically identical to the other mixing circuits except that three inputs were used (RF, LO and the undesired signal). The IF output was coupled to a device to measure the modulation envelope. Two methods were used to determine the percent cross-modulation on the IF carrier. In both methods, data were taken of the magnitude of undesired signal to yield 3% cross-modulation on the IF carrier.

The first method consisted of coupling the IF output into the first IF stage of a conventional receiver and measuring the detected audio output with an AC voltmeter. It was first necessary to modulate the RF at a known value, say 30% at 400 Hz; and observe the audio output. Since the system was considered linear, 1/30 of the voltmeter reading would indicate 3% modulation. The desired signal was then unmodulated, and the undesired signal (modulated at 30% and 400 Hz) was increased in amplitude until the voltmeter at the output indicated 3% modulation. The LO was held constant.

The second method consisted of coupling the IF output directly to a Singer Model SPA-3/25a Spectrum Analyzer. The 455 kHz pip was located on the CRT, and the bandwidth was reduced to zero so that only the envelope of the IF carrier appeared. With the analyzer reading on a linear scale it was fairly easy to measure 3% modulation.
The two methods of measurement yielded identical results. Since the spectrum analyzer method was the more straightforward of the two, it was used the majority of the time.
Fig. 52. Cross-modulation distortion test circuit.