Parameters of the Super-beta Transistor

Ho-An Au

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PARAMETERS OF THE SUPER-BETA TRANSISTOR

BY

HO-AN AU

A thesis submitted in partial fulfillment of the requirements for the degree Master of Science, Department of Electrical Engineering, South Dakota State University

1972
This thesis is approved as a creditable and independent investigation by a candidate for the degree, Master of Science, and is acceptable for meeting the thesis requirements for this degree. Acceptance of this thesis does not imply that the conclusions reached by the candidate are necessarily the conclusions of the major department.

Thesis Adviser

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CHAPTER I

INTRODUCTION

Transistors with current gains of 1,000 to 10,000 at collector current levels as low as 1 µA can now be made in discrete and in monolithic form. These devices are generally called super-beta or super-gain transistors.

It is well-known that a narrow base width results in a high-beta transistor. As the emitter is diffused more deeply into the base, reducing the base width, the current gain will increase. But there is a trade-off between breakdown voltage and current gain. When the emitter is deeply diffused, the depletion region of the collector-base junction may penetrate the base and reach through to the emitter, resulting in a collector-emitter short. However, by stopping the emitter diffusion in time, a super-beta transistor can be practically made.

The super-beta transistor has the disadvantage of collector-to-emitter voltage breakdown of less than 5.0 volts. This unusually low breakdown voltage precludes its use in standard circuit designs. However, it can be fabricated simultaneously with high-voltage transistors. It has been shown\(^1\) that circuit techniques are available, namely bootstrapping and cascode connections, that take advantage of the high-current gain of one transistor type and the high-breakdown voltage of the other, producing the equivalent of a high gain, high-voltage device.
This transistor is a new device. It has application in the first stage of an operational amplifier. The device requires low bias currents so the undesired output offset voltage can be minimized, and the high current gain can be important to minimize noise.

The goal of this research is to study the parameters of the super-beta transistor - dc characteristics, small signal behavior, large signal behavior, and noise - in order to better understand the device. Two types of super-beta transistors are used in this research. They are both discrete npn devices; type IT124 super-beta dual monolithic silicon planar transistor and type PR1 super-beta transistor. The IT124 is made by Intersil Incorporated and is available commercially; the type PR1 is a development sample produced by National Semiconductor.
2-1 Output Characteristics

Many different families of characteristic curves can be drawn, depending upon which two parameters are chosen as the independent variables. It is most useful to select the input and output voltages as the independent variables; then the input and output currents become the dependent variables. In Fig. 2-1, a super-beta transistor is shown in the grounded-emitter configuration. This circuit is also referred to as a common-emitter configuration, since the emitter is common to the input and output circuits. This configuration is used to measure the variables of the circuit. The potentiometer across the base voltage supply $V_{BB}$ is used to provide small variations in the base voltage. The base current is determined from calculation based upon $V_1$, $V_2$ and $R_B$, while the collector current is indicated by the ammeter.

$$I_C = I_B (1 + \frac{R_L}{R_B})$$

![Diagram](image) Fig. 2-1. Measurement circuit in common-emitter configuration.
Fig. 2-2 is the plot of collector current $I_C$ versus collector-to-emitter voltage $V_{CE}$ with base current $I_B$ as a parameter, for the type IT124 super-beta transistor. The curves of Fig. 2-2 are known as the output characteristics. Behavior in the active region is shown. In this region, the collector junction is biased in the reverse direction and the emitter junction in the forward direction. The values of the base current are in the range of nanoamperes, whereas the corresponding collector currents are in microamperes. The collector to emitter breakdown voltage is 2.0 V according to the manufacturer. Fig. 2-3 shows the output characteristics for higher values of base current. Since this transistor is operated at low current levels, the curve-tracer which is designed for general bipolar transistors can not be used to study the characteristics of this kind of transistor. Figs. 2-4 and 2-5 show the output characteristic curves of a sample of type PR1 super-beta transistor.

2-2 Input Characteristics

In Fig. 2-6 the abscissa is the base-to-emitter voltage $V_{BE}$ and the ordinate is the base current $I_B$. The data are given for various values of collector-to-emitter voltage $V_{CE}$. This is the input characteristic of the type IT124 super-beta transistor. For any value of $V_{CE}$, the base current $I_B$ for small $V_{BE}$ is approximately zero. This value is too small to be observed. A noteworthy feature of the input characteristics is that there exits a cut-in voltage, below which the base current is negligible. In Fig. 2-6, we find that the cut-in voltage is approximately 0.35 V at the conditions $V_{CE} = 1.0$ V, $I_C = 10$
Fig. 2-2. The output characteristics of type IT124 unit.

Fig. 2-3. The output characteristics of type IT124 unit with higher base current.
Fig. 2-4. The output characteristics of type PR1 unit.

Fig. 2-5. The output characteristics of type PR1 unit with higher base current.
Fig. 2-6. The input characteristics of type IT124 unit.

Fig. 2-7. The input characteristics of type IT124 unit with higher base current.
μA. Also from the graph, we can determine the dc input resistance of the transistor, which is about 2.56 MΩ at $V_{CE} = 1.0 \text{ V}$, $I_C = 100 \mu\text{A}$.

Higher base currents are shown in Fig. 2-7. The cut-in voltage is 0.715 V at the conditions $V_{CE} = 1.1 \text{ V}$, $I_C = 1.0 \text{ mA}$. The input resistance is 2.59 MΩ at $V_{CE} = 1.1 \text{ V}$, $I_C = 1.3 \text{ mA}$. Figs. 2-8 and 2-9 show the input characteristics of type PR1 super-beta transistor for other base current values. In Fig. 2-8, the cut-in voltage is approximately 0.33 V at the conditions $V_{CE} = 1.0 \text{ V}$, $I_C = 10 \mu\text{A}$; the dc input resistance is 3.44 MΩ at $V_{CE} = 1.0 \text{ V}$, $I_C = 100 \mu\text{A}$. At the higher base current, the cut-in voltage is 0.636 V at $V_{CE} = 1.1 \text{ V}$, $I_C = 1.0 \text{ mA}$; the input resistance is 2.6 MΩ at $V_{CE} = 1.1 \text{ V}$, $I_C = 1.3 \text{ mA}$.

2-3 The DC Current Gain $h_{FE}$

A transistor parameter of interest is the ratio $I_C/I_B$, where $I_C$ is the collector current and $I_B$ is the base current. This quantity is designated by $\beta_{dc}$ or $h_{FE}$, and is known as the dc beta, or the dc current gain.

Figs. 2-10 and 2-11 show the dc current gain versus collector current for the type IT124 and PR1 devices, respectively. At the conditions $V_{CE} = 1.0 \text{ V}$, $I_C = 100 \mu\text{A}$, we find that the dc current gain $h_{FE}$ of the type IT124 is 2360, whereas for the type PR1 it is 3370. These values are larger than those of bipolar transistors. The values of $h_{FE}$ are different for distinct $V_{CE}$ values. The variation of $h_{FE}$ with collector current for type IT124 and PR1 samples are shown in Figs. 2-12 and 2-13. For both of these transistors, the dc current gain falls off as the collector current increases. At $V_{CE} = 1.1 \text{ V}$, $I_C = 1.0 \text{ mA}$,
Fig. 2-8. The input characteristics of type PR1 unit.

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Fig. 2-13. Plot of dc current gain $h_{FE}$ vs. higher collector current for different $V_{CE}$ of the type PR1 unit.
The dc current gain of the type IT124 unit drops down to 336. It is clear that when this transistor is operated under lower collector-to-emitter voltages, or at higher collector currents, it no longer behaves as a super-beta transistor. The dc current gain of the type PR1 is 3220 at $V_{CE} = 1.1$ V, $I_C = 1.0$ mA.
CHAPTER III

SMALL SIGNAL BEHAVIOR

Under small signal conditions, where the variations about the quiescent point are assumed small, circuit models are used to study the behavior of the transistors. The set of hybrid parameters is used to represent the super-beta transistor in this chapter. The major reasons we use this model are: the parameters are real numbers at audio-frequencies, they are easy to measure, they can be obtained from the transistor static characteristic curves, and they are particularly convenient to use in circuit analysis and design.

3-1 Definition of h Parameters

The terminal behavior of two-port devices may be specified by two voltages and two currents. The box in Fig. 3-1 represents such a two-port network. If the current \( I_1 \) and the voltage \( V_2 \) are independent and if the two-port is linear, we may write

\[
V_1 = h_{11}I_1 + h_{12}V_2 \quad (3-1)
\]

\[
I_2 = h_{21}I_1 + h_{22}V_2 \quad (3-2)
\]

The quantities \( h_{11}, h_{12}, h_{21}, \) and \( h_{22} \) are called the \( h \) or hybrid parameters because they are not all alike dimensionally. Let us assume that there are no reactive elements within the two-port network. Then from Eqs. (3-1) and (3-2), the \( h \) parameters are defined as follows:

\[
h_{11} = \left. \frac{V_1}{I_1} \right|_{V_2 = 0} \quad \text{input resistance with output short-circuited (ohms).}
\]
\[ h_{12} = \left| \frac{V_1}{V_2} \right|_{I_1 = 0} = \text{fraction of output voltage at input with input open-circuited, or more simply, reverse-open-circuit voltage amplification (dimensionless).} \]

\[ h_{21} = \left| \frac{I_2}{I_1} \right|_{V_2 = 0} = \text{negative of current transfer ratio with output short-circuited. This parameter is usually referred to as the short-circuited current gain (dimensionless).} \]

\[ h_{22} = \left| \frac{I_2}{V_2} \right|_{I_1 = 0} = \text{output conductance with input open-circuited (mhos).} \]

The following convenient alternative subscript notation is recommended by the IEEE Standards:

\[ i = 11 = \text{input impedance} \quad o = 22 = \text{output admittance} \]

\[ f = 21 = \text{forward transfer} \quad r = 12 = \text{reverse transfer} \]

In the case of transistors, another subscript \((b, e, \text{or } c)\) is added to designate the configuration.

Since the device described by Eqs. (3-1) and (3-2) is assumed to include no reactive elements, the four parameters \(h_{11}, h_{12}, h_{21}, \text{and } h_{22}\) are real numbers, and the voltages and currents \(V_1, V_2, \text{and } I_1, I_2\) are function of time.

We may now use the four \(h\) parameters to construct a mathematical model of the device of Fig. 3-1. The hybrid circuit for any device characterized by Eqs. (3-1) and (3-2) is indicated in Fig. 3-2. We can verify that the model of Fig. 3-2 satisfies Eqs. (3-1) and (3-2) by
Fig. 3-1. A two-port network.

Fig. 3-2. The hybrid model for the two-port network of Fig. 3-1.

\[ V_b = h_{ie} I_b + h_{re} V_c \]
\[ I_c = h_{fe} I_b + h_{oe} V_c \]

Fig. 3-3. Common-emitter hybrid model and its v-i equation.
writing Kirchhoff's voltage and current laws for the input and output ports, respectively.

Here the common-emitter configuration is used; the hybrid model and the terminal v-i equations are shown in Fig. 3-3.

3-2 Determination of the h Parameters from the Characteristics

We can determine the h parameters graphically from the transistor characteristic curves. Let us introduce a set of equations:

\[ h_{ie} = \frac{\Delta v_B}{\Delta i_B} \mid V_C \]
\[ h_{re} = \frac{\Delta v_B}{\Delta v_C} \mid I_B \]
\[ h_{fe} = \frac{\Delta i_C}{\Delta i_B} \mid V_C \]
\[ h_{oe} = \frac{\Delta i_C}{\Delta v_C} \mid I_B \]

The above equations give the form of the functional relationships for the common-emitter connection of total instantaneous collector current and base voltage in terms of two variables, namely, base current and collector voltage. Such functional relationships are represented by families of characteristic curves. Two families of curves are usually specified for transistors. The output characteristic curves depict the relationship between output current and voltage, with input current as the parameter. The input characteristics depict the relationship between input voltage and current with output voltage as the parameter.

If the input and output characteristics of a particular connection are given, the h parameters can be determined graphically. For a common-emitter configuration, the output and input characteristic curves are shown in Figs. 3-4 and 3-5, respectively.
Fig. 3-4. CE output characteristics - determination of $h_{fe}$ and $h_{oe}$.

Fig. 3-5. CE input characteristics - determination of $h_{ie}$ and $h_{re}$. 
(a) \( h_{fe} = \frac{\Delta i_C}{\Delta i_B} \frac{1}{V_C} = \frac{i_{C2} - i_{C1}}{i_{B2} - i_{B1}} \)

The current increments are taken around the quiescent point \( Q \), which corresponds to base current \( i_B = I_B \) and to the collector voltage \( V_{CE} = V_C \).

(b) \( h_{oe} = \frac{\Delta i_C}{\Delta V_C} \frac{1}{I_B} \)

The value of \( h_{oe} \) at the quiescent point \( Q \) is given by the slope of the output characteristic curve at that point. This shape can be evaluated by drawing the line \( AB \) in Fig. 3-4 tangent to the characteristic curve at the point \( Q \).

(c) \( h_{ie} = \frac{\Delta V_B}{\Delta i_B} \frac{1}{V_C} \)

Hence the slope of the appropriate input characteristic at the quiescent point \( Q \) gives \( h_{ie} \). In Fig. 3-5, \( h_{ie} \) is given by the slope of the line \( EF \), which is drawn tangent to the characteristic curves at the point \( Q \).

(d) \( h_{re} = \frac{\Delta V_B}{\Delta V_C} \frac{1}{I_B} = \frac{V_{B2} - V_{B1}}{V_{C2} - V_{C1}} \)

A vertical line on the input characteristics of Fig. 3-5 represents constant base current. The parameter \( h_{re} \) can now be obtained as the change in base voltage, \( V_{B2} - V_{B1} \), divided by the change in collector voltage, \( V_{C2} - V_{C1} \), for a constant base current \( I_B \), at the quiescent point \( Q \). Since \( h_{re} \approx 10^{-4} \), then \( v_B \ll v_C \), and the above method, although correct in principle, it is very inaccurate in practice.

The method discussed above yields an estimation of the \( h \) parameters of a transistor. Now we will use this method to estimate the \( h \) para-
meters of super-beta transistors at several quiescent points. For common-emitter connected IT124 and PR1 super-beta transistors, the characteristics are shown in Fig. 2-2 through Fig. 2-9. According to the method discussed above, we find that the h parameters of type IT124 super-beta transistor at \( V_C = 1.0 \, V \), \( I_C = 0.10 \, mA \) are

\[
\begin{align*}
  h_{ie} &= 5.7 \times 10^6 \, \Omega \\
  h_{oe} &= 80 \times 10^{-6} \, \text{mho}
\end{align*}
\]

\( h_{ie} = 5.7 \times 10^3 \)

While at \( V_C = 1.1 \, V \), \( I_C = 1.0 \, mA \)

\[
\begin{align*}
  h_{ie} &= 6 \times 10^3 \, \Omega \\
  h_{oe} &= 0.95 \times 10^{-3} \, \text{mho}
\end{align*}
\]

\( h_{ie} = 70 \)

For type PR1 at \( V_C = 1.0 \, V \), \( I_C = 0.10 \, mA \)

\[
\begin{align*}
  h_{ie} &= 3.3 \times 10^6 \, \Omega \\
  h_{oe} &= 1.1 \times 10^{-6} \, \text{mho}
\end{align*}
\]

\( h_{ie} = 3.84 \times 10^3 \)

While at \( V_C = 1.1 \, V \), \( I_C = 1.0 \, mA \)

\[
\begin{align*}
  h_{ie} &= 0.1 \times 10^6 \, \Omega \\
  h_{oe} &= 0.2 \times 10^{-3} \, \text{mho}
\end{align*}
\]

\( h_{ie} = 2.66 \times 10^3 \)

3-3 Measurement of h Parameters

h parameters of a super-beta transistor can be determined either graphically or from laboratory measurements. Graphical determination, as mentioned in the previous section, is not highly accurate. The "BIRTCHER Semiconductor Test Set Model 70" is available to measure the h parameters of a conventional transistor directly. The input signal voltage of this instrument to the test device is 1 V peak-to-peak, and since this is too large for a super-beta transistor, we can not use the test set. Based on the definition given in Sec. 3-1, a simple
experimental circuit may be assembled for the direct measurement of the hybrid parameters. Consider the circuit of Fig. 3-6. The desired quiescent conditions are obtained from adjustable supplies \( V_{CC} \) and \( V_{BB} \). The reactance of \( C_1 \) and \( C_2 \) are negligible at the frequency of the sinusoidal generator, 1 kHz. We may consider the super-beta transistor output port to be short-circuited to the signal.

Note that we now use capital letters to represent phasor rms voltages and currents. Hence \( \Delta V_B', \Delta i_B', \Delta V_c \) and \( \Delta i_c \) of the preceding section are replaced by \( V_b, I_b, V_c \) and \( I_c \), respectively. The input signal voltage to the super-beta transistor is measured by a voltmeter between base and emitter. We may consider the signal-input current to be

\[
I_b = \frac{V'_s - V_b}{R_1} - I_b'
\]

where \( V'_s \) is the voltage measured across \( R_B \) and \( I_b' \) is the current flowing through the voltmeter which is located across the base and emitter.

The value of \( h_{ie} \) is given

\[
h_{ie} = \left. \frac{V_b}{I_b} \right|_{V_c = 0} = \frac{V_s'}{V_b \left( \frac{V'_s - V_b}{R_1} - I_b' \right)}
\]

Hence the input resistance \( h_{ie} \) may be calculated from the two measured voltages \( V'_s \) and \( V_b \).

The circuit of Fig. 3-7 is used to measure \( h_{fe} \). This circuit is the same as in Fig. 3-6, except \( R_E \) is inserted between the emitter and ground in order to determine the collector signal current. Since \( R_E \) is 100\( \Omega \), we may consider the configuration as common-emitter circuit.
Fig. 3-6. Circuit for measuring $h_{ie}$.

Fig. 3-7. Circuit for measuring $h_{fe}$. 
The emitter signal current is determined by $\frac{V_o}{R_E}$, which is almost the same as collector signal current.

For parameter $h_{fe}$ is given by

$$h_{fe} = \frac{I_C}{I_B} \bigg|_{V_C = 0} = \frac{V_o R_1}{R_E V_s}$$

Thus $h_{fe}$ is obtained from the two measured voltages $V_s'$ and $V_o$.

The circuit of Fig. 3-8 may be used to measure $h_{re}$. The signal now is applied to the collector directly through a capacitor which is used to block the dc current from supply $V_{cc}$. Because we select $R_1 = 100 \, M\Omega$ which is large compared with the input resistance of the super-beta transistor, the base circuit may be considered effectively open-circuited as far as the signal is concerned.

We then obtain

$$h_{re} = \frac{V_b}{V_c} \bigg|_{I_B = 0} = \frac{V_b}{V_c}$$

$V_b$ is measured across $R_1$, and $V_c$ is measured at the collector.

Consider the circuit of Fig. 3-9. It is used to measure the $h_{oe}$ parameter. If $R_B = 10 \, M\Omega$ which is large compared with $R_i$, the base circuit may be considered effectively open-circuited as far as the signal is concerned. The collector current is determined from $R_E$.

The output conductance is

$$h_{oe} = \frac{I_C}{V_C} \bigg|_{I_B = 0} = \frac{V_o}{R_E V_c}$$

Hence $h_{oe}$ is obtained from the measured voltages $V_o$ and $V_c$.

In measuring $V_o$ and $V_b$, it is necessary for the reading to be
Fig. 3-8. Circuit for measuring $h_{re}$.

Fig. 3-9. Circuit for measuring $h_{oe}$. 
smaller than 0.5 mV when there is no signal input to the circuit. This will assure the accuracy of the readings. The values of $R_1$ and $R_E$ which are used to determine the currents should be within ±1% tolerance in order for the error to be limited to 1 percent.

3-4 Experimental Data

Using the circuits as discussed in the previous section, we obtained the $h$ parameters of the super-beta transistors. They are listed in the following tables for different types and bias conditions. Table 3-1 shows the $h$ parameters of IT124 super-beta transistor and Table 3-2 shows the $h$ parameters of PR1 super-beta transistor.

From this data, we found that the super-beta transistors have high values of short-circuit current gain, ten or more times greater than conventional bipolar transistors. This is why they are called super-beta or super-gain transistors. For type IT124, the value of $h_{fe}$ reaches 1644 at the bias conditions $V_C = 1.0 \, V, I_C = 0.2 \, mA$. It becomes 814 when $I_C$ is equal to 1.0 mA. Type PR1 has higher beta value than type IT124. The value is as high as 3220 when $V_C = 1.0 \, V, I_C = 0.2 \, mA$, while at $I_C = 1.0 \, mA$, it only has decreased to 2520. Besides the high value of current gain, this type also has higher input resistance $h_{ie}$. Both of these two super-beta transistors have about 1 MΩ input resistance at $V_C = 1.0 \, V, I_C = 0.02 \, mA$. Also type PR1 has a higher value of $h_{ie}$ than type IT124.

Now let us measure the parameters of a type 2N956 bipolar transistor with the "BIRCHER Semiconductor Test Set". We find the $h$ parameters of this transistor under bias conditions $V_C = 5.0 \, V, I_C = 1.0 \, mA
### TABLE 3-1

$h$ parameter values of type IT124 super-beta transistor (at $V_C = 1.0 \, \text{V}, \, f = 1 \, \text{kHz}$).

<table>
<thead>
<tr>
<th>$I_C$ (mA)</th>
<th>$h_{fe}(x10^3)$</th>
<th>$h_{le}(x10^5)$</th>
<th>$h_{oe}(x10^{-6})$</th>
<th>$h_{re}(x10^{-3})$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.02</td>
<td>1.168</td>
<td>12.85</td>
<td>15.32</td>
<td>10.7</td>
</tr>
<tr>
<td>0.04</td>
<td>1.42</td>
<td>9.82</td>
<td>19.8</td>
<td>9.18</td>
</tr>
<tr>
<td>0.06</td>
<td>1.538</td>
<td>7.8</td>
<td>22.9</td>
<td>8.21</td>
</tr>
<tr>
<td>0.08</td>
<td>1.545</td>
<td>6.24</td>
<td>26.1</td>
<td>7.41</td>
</tr>
<tr>
<td>0.10</td>
<td>1.640</td>
<td>5.21</td>
<td>29.5</td>
<td>6.74</td>
</tr>
<tr>
<td>0.20</td>
<td>1.644</td>
<td>2.81</td>
<td>45.6</td>
<td>4.83</td>
</tr>
<tr>
<td>0.40</td>
<td>1.37</td>
<td>1.28</td>
<td>100.0</td>
<td>2.92</td>
</tr>
<tr>
<td>0.60</td>
<td>0.462</td>
<td>0.671</td>
<td>415.0</td>
<td>1.47</td>
</tr>
<tr>
<td>0.80</td>
<td>0.153</td>
<td>0.270</td>
<td>622.4</td>
<td>1.29</td>
</tr>
<tr>
<td>1.0</td>
<td>0.0814</td>
<td>0.112</td>
<td>791.0</td>
<td>0.858</td>
</tr>
</tbody>
</table>

### TABLE 3-2

$h$ parameter values of type PR1 super-beta transistor (at $V_C = 1.0 \, \text{V}, \, f = 1 \, \text{kHz}$).

<table>
<thead>
<tr>
<th>$I_C$ (mA)</th>
<th>$h_{fe}(x10^3)$</th>
<th>$h_{le}(x10^5)$</th>
<th>$h_{oe}(x10^{-6})$</th>
<th>$h_{re}(x10^{-3})$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.02</td>
<td>2.25</td>
<td>15.4</td>
<td>28.5</td>
<td>12.2</td>
</tr>
<tr>
<td>0.04</td>
<td>2.76</td>
<td>13.7</td>
<td>36.5</td>
<td>11.2</td>
</tr>
<tr>
<td>0.06</td>
<td>2.94</td>
<td>11.9</td>
<td>42.1</td>
<td>10.3</td>
</tr>
<tr>
<td>0.08</td>
<td>3.07</td>
<td>10.6</td>
<td>45.4</td>
<td>9.49</td>
</tr>
<tr>
<td>0.10</td>
<td>3.14</td>
<td>9.32</td>
<td>50.0</td>
<td>8.85</td>
</tr>
<tr>
<td>0.20</td>
<td>3.22</td>
<td>5.23</td>
<td>67.1</td>
<td>6.56</td>
</tr>
<tr>
<td>0.40</td>
<td>3.06</td>
<td>2.55</td>
<td>113.1</td>
<td>3.76</td>
</tr>
<tr>
<td>0.60</td>
<td>2.88</td>
<td>1.61</td>
<td>156.1</td>
<td>2.19</td>
</tr>
<tr>
<td>0.80</td>
<td>2.74</td>
<td>1.16</td>
<td>206.0</td>
<td>2.12</td>
</tr>
<tr>
<td>1.0</td>
<td>2.52</td>
<td>0.902</td>
<td>261.0</td>
<td>2.94</td>
</tr>
</tbody>
</table>
to be:

\[ h_{fe} = 111 \quad h_{le} = 3260 \, \Omega \]

\[ h_{oe} = 19.6 \times 10^{-5} \, \text{mho} \quad h_{re} = 5.5 \times 10^{-4} \]

Let us compare these values with the PR1 super-beta transistor at \( I_C = 0.10 \, \text{mA} \). We find that the value of \( h_{fe} \) of PR1 super-beta transistor is about thirty times larger. The input resistance of the super-beta transistor is much much larger than that of bipolar transistor, about one hundred times larger. The output conductance \( h_{oe} \), has a larger value for the super-beta transistor, but the difference is not very significant. The parameter \( h_{re} \) is about ten times larger for the super-beta transistor. This high value means a larger amount of feedback of the output voltage to the input terminal; this is undesirable.

3-5 Hybrid-parameter Variations

The values of the \( h \) parameters not only depend upon the operating point, but also depend on the ambient temperature. Only the variation in \( h \) parameters with collector current is discussed in this section. We compare the super-beta transistor with the bipolar transistor.

From the discussion in Sec. 3-2 we have seen that once a quiescent point \( Q \) is specified, the \( h \) parameters can be obtained from the characteristic curves. Since the characteristic curves are not equally spaced for equal changes in \( I_B \) or \( V_{CE} \), it is clear that the values of the \( h \) parameters depend upon the location of the quiescent point. Such curves are shown for IT124 and PR1 super-beta transistors in Figs. 3-10 and 3-11. Data for these curves were obtained by using the circuits in Fig. 3-6 through Fig. 3-9, and they were also listed in Table 3-1 and 3-2.
Fig. 3-10. Parameter variations with $I_C(Q)$ of IT124.

Fig. 3-11. Parameter variations with $I_C(Q)$ of PR1.
Fig. 3-12 shows the typical variations of h parameters of a bipolar transistor with collector current. Both the super-beta transistor and the bipolar transistor behave similarly when we consider $h_{oe}$ and $h_{ie}$. When considering $h_{fe}$ and $h_{re}$, these two different types of transistors behave oppositely. Instead of increasing with collector current, the parameters of the super-beta transistor decrease with an increase in collector current.

3-6 High Frequency h Parameters

The parameters of some transistor types begin to take on complex form at frequencies beyond the upper end of the audiofrequency spectrum. Low frequency parameters are simply real numbers; for high frequency analysis, the parameters also have reactive portions that represent physical capacitance effects and the distributed nature of some of the internal functions.

Because of the diffusion capacitance, the magnitude of the common-base current amplification factor $h_{fb}$ is found to vary with frequency according to the approximate relation

$$h_{fb} = \frac{h_{fb0}}{1 + j(f/f_{hfb})}$$

(3-3)

$f_{hfb}$ is referred to as the alpha-cutoff frequency. At the cutoff frequency, $h_{fb}$ has decreased to 0.707 of its reference value.

In this section common-emitter operation is considered. We are interested in $h_{fe}$; $h_{fe}$ is a function of $h_{fb}$, and has the following relation

$$h_{fe} = \frac{-h_{fb}}{1 + h_{fb}}$$

(3-4)
Fig. 3-12. Parameter variations with $I_C(Q)$ of a typical transistor.

Fig. 3-13. Circuit for measuring $h_{fe}$ at higher frequency.
Therefore upon substitution of Eq. (3-3) into Eq. (3-4) we obtain

\[
h_{fe} = \frac{h_{feo}}{1 + j(f/f_{hfe})}
\]  

where \( f_{hfe} = (1 + h_{fbo})f_{hf} \), is referred to as the beta-cutoff frequency; it is also symbolized by \( f_\beta \). When \( f = f_\beta \), \(|h_{fe}|\) is reduced to \( \sqrt{2} / 2 \) times its low frequency value \( h_{feo} \); therefore \( f_\beta \) serves as a useful measure of the band of frequencies over which the current gain remains reasonably constant.

Consider the circuit of Fig. 3-13. This circuit is slightly different from that circuit shown in Fig. 3-7. A 0.01 \( \mu \)F non-electrolytic capacitor parallels a 10 \( \mu \)F electrolytic capacitor as the ac short-circuit. A non-electrolytic capacitor is used to provide a good ac short-circuit at high frequencies. The base current is determined by

\[
I_b = \frac{V_s' - V_b}{R_1} - \frac{V_b}{R_{in}}
\]

where \( R_{in} \) is the input resistance of the voltmeter. The collector current is determined from \( V_o / 100 \). From these two currents we can obtain the values of \( h_{fe} \).

Fig. 3-14 shows the variation of \( h_{fe} \) of type IT124 super-beta transistor versus frequency, operating at \( V_{CE} = 1.0 \) V, \( I_C = 0.1 \) mA, and Fig. 3-15 shows the variation of \( h_{fe} \) of another type PR1 super-beta transistor versus frequency, operating at the same point. It is clear from the graph that the values of \( h_{fe} \) decrease when frequency increases. The dotted line shows the calculated values. First we determined the beta cutoff frequency from the experimental data, where the \( h_{fe} \) value drops down to 0.707 of its low-frequency value, and then calculated \( h_{fe} \).
Fig. 3-14. The short-circuit CE current gain vs.
frequency of IT124.

Fig. 3-15. The short-circuit CE current gain vs.
frequency of PR1.
by using Eq. (3-5). Then we plot the normalized value on the graph. The experimental and calculated curves for both super-beta transistors are in good agreement, but the experimental rates of decrease at high frequencies are smaller than the calculated curves. The beta-cutoff frequency of type IT124 super-beta transistor is 4.0 kHz, while for type PR1 it is 1.3 kHz. We know that the general-purpose bipolar transistors have values of $f_B$ in the range of 10 kHz. Since the beta-cutoff frequencies of these two types are quite low, they are not suitable to be used in high frequency operation.

At high frequencies, the collector and diffusion capacitances are the factors that result in operational differences. They are not constant, but are subject to variations due to temperature, emitter current, collector potential, frequency and manufacturing techniques. Figs. 3-16 and 3-17 show the values of $h_{fe}$ as a function of frequency for the two different types of super-beta transistors, operating under different bias conditions. Both of these experimental curves have smaller rates of decrease than the calculated curves. For type IT124 super-beta transistor, the cutoff frequency is changed to 10 kHz, while for type PR1, the cutoff frequency is changed to 5.3 kHz. Fig. 3-18 shows the value of $h_{fe}$ as a function of frequency for type IT124 super-beta transistor, operating at $V_C = 1.0 \, V$, and a higher collector current, $I_C = 0.4 \, mA$. Not only is the beta cutoff frequency higher, but there is a peak at about 4 kHz. Fig. 3-19 shows the value of $h_{fe}$ as a function of frequency for the type PR1 super-beta transistor, operating at $V_C = 1.0 \, V$, $I_C = 1.1 \, mA$, also at a higher collector current. The beta cutoff frequency increases, and the values of
Fig. 3-16. The short-circuit CE current gain vs. frequency at different collector current of IT124.

Fig. 3-17. The short-circuit CE current gain vs. frequency at different collector current of PR1.
Fig. 3-18. The short-circuit CE current gain vs. frequency at higher collector current of IT124.

Fig. 3-19. The short-circuit CE current gain vs. frequency at higher collector current of PR1.
$h_{fe}$ are a little bit higher at about 1 kHz.

3-7 Transconductance $g_m$

The super-beta transistor has a higher input resistance than the bipolar transistor. The vacuum tube has very high input resistance and transconductance $g_m$ is used to represent its gain characteristics. Therefore, in this section we investigate the $g_m$ parameter of the super-beta transistor. Fig. 3-20 shows the hybrid-$\pi$ model of a transistor. Assume that the collector and emitter are short-circuited, and the signal frequency is 1 kHz. The approximate equivalent circuit useful to calculate the short-circuited current gain is shown in Fig. 3-21.

$g_m$ is determined by

$$g_m = \frac{I_o}{V_{b'e}}$$

The circuit in Fig. 3-22 shows the set-up used to measure the $g_m$ of the super-beta transistor. Two capacitors are connected across the $V_{CC}$ power supply. Since the value of $R_L$ is small, we may consider the load to be a short circuit. The $g_m$ value can be determined from measurement of voltages $V_o$ and $V_{be}$. Actually the transconductance determined from this circuit is not identical to defined transconductance for transistors, because the voltage measured between the base and emitter is not $V_{b'e}$. We designate this measured value by $g_m'$.

Fig. 3-23 shows the $g_m'$ values as a function of frequency for the both types IT124 and PR1 super-beta transistors, at the same bias conditions $V_{CE} = 1.0$ V, $I_C = 0.4$ mA. Type PR1 has larger $g_m'$ value than type IT124. The $g_m'$ value of type PR1 remains constant until...
Fig. 3-20. Hybrid-\( \pi \) model of a transistor.

Fig. 3-21. Approximate equivalent circuit for the calculation of the short-circuit CE current gain.

Fig. 3-22. Circuit for measuring \( g_m' \).
Fig. 3-23. Transconductance $g_m'$ vs. frequency of the super-beta transistors.

$V_C = 1.0 \, V, \, I_C = 0.4 \, mA$
2 MHz, and drops down to 0.707 of its low frequency values at 10 MHz. But the $g_m'$ value of type IT124 remains constant until 6 MHz, and decreases to 0.707 of its low frequency values at about 19.5 MHz, which is higher than that of type PR1 super-beta transistor.

Fig. 3-24 shows the phase angles of the $g_m'$ values of these two types of transistors versus frequency. Both of these two types of transistors have 180 degrees phase angle at low frequency. The phase angles start to fall off beyond 1 MHz, and decrease to around 110 degrees at 50 MHz. At cutoff frequency, the phase angle is 136 degrees for type IT124, while for type PR1 the phase angle is 152 degrees.

3-8 Analysis of a Super-beta Transistor Amplifier Circuit using h Parameters

To form a transistor amplifier it is only necessary to connect an external load and signal source as indicated in Fig. 3-25 and to bias the transistor properly. The two-port active network of Fig. 3-25 represents a transistor in any one of the three possible configurations. In Fig. 3-26 we show the small signal hybrid model for a common-emitter connection. The circuit used in Fig. 3-26 is valid for any type of load whether it be a pure resistance, an impedance, or another transistor. This is true because the transistor hybrid model was derived without any regard to the external circuit in which the transistor is incorporated. The only restriction is the requirement that the h parameters remain substantially constant over the operating range. Here a pure resistance load is considered.

Assuming sinusoidally varying voltages and currents, we can proceed
Fig. 3-24. Phase angle of \( g_m' \) vs. frequency.

Fig. 3-25. A basic amplifier circuit.

Fig. 3-26. Small signal hybrid model for a common-emitter amplifier circuit.
with the analysis of the circuit of Fig. 3-26, using the phasor notation to represent the sinusoidally varying quantities. The quantities of interest are the current gain, the input resistance, the voltage gain, and the output resistance.

Now let us take a set of \( h \) parameters from Table 3-1. At \( V_C = 1.0 \) \( V, I_C = 0.10 \) mA, the \( h \) parameters of type IT124 super-beta transistor are:

\[
\begin{align*}
h_{fe} &= 1.640 \times 10^3 \\
h_{oe} &= 29.5 \times 10^{-6} \text{ mho}
\end{align*}
\]

Using this set of values we may calculate \( A_v, A_i, R_i \) and \( R_o \). If \( R_L = 10 \, k\Omega, R_S = 600\Omega \), we found that:

\[
\begin{align*}
A_v &= \frac{-h_{fe}R_L}{h_{ie} + R_L} = -30.9 \\
A_i &= \frac{h_{fe}}{1 + h_{oe}R_L} = 1268 \\
R_i &= \frac{h_{ie} + R_L}{1 + h_{oe}R_L} = 409 \times 10^3 \Omega \\
R_o &= \frac{h_{ie} + R_S}{h_{oe} + R_S} = 133 \times 10^3 \Omega
\end{align*}
\]

For type PR1 super-beta transistor, the values of \( h \) parameters from Table 3-2 at \( V_C = 1.0 \) \( V, I_C = 0.10 \) mA are

\[
\begin{align*}
h_{fe} &= 3.14 \times 10^3 \\
h_{oe} &= 50.0 \times 10^{-6} \text{ mho}
\end{align*}
\]

Then

\[
\begin{align*}
A_v &= -31.3 \\
A_i &= 2090 \\
R_i &= 667 \times 10^3 \Omega \\
R_o &= 57.4 \times 10^3 \Omega
\end{align*}
\]
From the above calculated values, we concluded that both types of super-beta transistors have appropriate voltage gain, very high current gain, and high input and output resistances. As compared with the bipolar transistor, we may say that the super-beta transistor has very high current gain, high input and output resistances.

3-9 Discussion of Voltage Gain

In the laboratory, there are many excellent instruments available for measuring signal voltage, whereas there are no instruments that are completely satisfactory for measuring signal currents. Therefore, of the four interested quantities, voltage gain, current gain, input resistance and output resistance, discussed in the previous section, only voltage gain is considered in this section.

Fig. 3-27 shows the voltage gain as a function of the dc collector current of type IT124 super-beta transistor in a simple amplifier circuit. Data for two different load resistances are plotted on the graph. The values of voltage gain increase with the collector current, and reach a maximum value around 0.40 mA collector current. The dashed curves are calculated values by using the known h parameters and load resistance values. These two experimental and calculated curves are in good agreement.

Fig. 3-28 shows the voltage gain as a function of collector current for type PR1 super-beta transistor in the simple amplifier circuit. We find that the experimental and calculated curves are in better agreement for the smaller load resistance.

Fig. 3-29 shows the voltage gain of a type IT124 super-beta
Fig. 3-27. Voltage gain vs. collector current of IT124.

Fig. 3-28. Voltage gain vs. collector current of PR1.
Fig. 3-29. Voltage gain vs. frequency of the type IT124 super-beta transistor.
Fig. 3-30. Voltage gain vs. frequency of the type PR1 super-beta transistor.
sistor simple amplifier circuit as a function of frequency. Data for two different load resistances as well as two different collector currents are plotted on the graph. For larger load resistance, the cutoff frequency of the voltage gain is about 230 kHz. But for smaller load resistance, the cutoff frequency is 480 kHz.

Fig. 3-30 shows the voltage gain of type PR1 super-beta transistor simple amplifier circuit as a function of frequency. Also the data for two different load resistances as well as two different dc collector currents are plotted on the graph. The cutoff frequencies of the voltage gain of this type transistor are the same as type IT124. It is about 230 kHz for larger load resistance and about 480 kHz for smaller load resistance.
When a device is operated with a large-signal input, the assumptions of linear operation are no longer valid. For accurate analysis, a graphical method is often used. Since the super-beta transistor must be operated at very low power supply voltage, it is not suitable to be used as a power amplifier. In this chapter we discuss the response of the super-beta transistor to large signals. The voltage transfer characteristics are studied, and the device is compared with the bipolar transistor. The simple large-signal audiofrequency amplifier operating at 1 kHz is considered in this chapter.

4-1 Graphical Analysis of the Super-Beta Transistor Amplifier

Graphical analysis of the super-beta transistor amplifier provides an insight into the large signal performance of the amplifier. The circuit diagram for a super-beta transistor amplifier is shown in Fig. 4-1. The bias voltage $V_{BB}$ is included in the circuit to allow class A operation. Since the input signal voltage at the base of the transistor must be quite small, a voltage divider is needed to decrease the signal voltage $V_s$.

First let us examine the output collector characteristic as shown in Fig. 4-2. A static load line is drawn on the curve with the slope of $\tan^{-1}(1/R_L)$. The projection of the extreme of the operating range on the abscissa gives the maximum peak-to-peak value of the output voltage, while the projection on the ordinate gives the maximum peak-
Fig. 4-1. A simple amplifier circuit.

Fig. 4-2. Collector characteristics.
to-peak value of the output current. The portion of the load line between saturation and cutoff regions is called the active region of the amplifier; in this region the super-beta transistor amplifies the input signal. The operating point must be situated somewhere within the active region on the load line. Let us consider the operating point that is located right in the middle of the operating range so that we have a class A amplifier. For small signals, the output voltage is a reasonably good reproduction of the input-signal waveform. When the input signal increases, the output signal voltage as well as the output current reach the cut-off and saturation regions. Then the signal waveform is clipped, and the amplifier circuit does not reproduce the original waveform faithfully. The gain of the amplifier decreases.

4-2 Voltage Transfer Characteristics

When the output voltage is plotted as a function of the input voltage, we have a voltage transfer characteristic. Fig. 4-3 shows the ideal voltage transfer characteristic of a simple amplifier circuit. The construction shows how the transfer characteristic can be used to determine the waveform of the output voltage when the waveform of the input voltage is as shown. Points A and B are the boundaries of the active linear region; saturation and cutoff regions are also shown. Distortionless amplification requires a linear transfer characteristic, and the slope of this linear region determines the gain of the amplifier. It is clear that under large signal operating conditions, the curvature of the characteristic flattens the peak and exaggerates the valley in the waveform of the output voltage. Also from the graph we
Fig. 4-3. Voltage transfer characteristic.
can note the collector to emitter saturation voltage \( V_{CE}^{\text{(sat)}} \) and the power supply voltage \( V_{CC} \).

Fig. 4-4 shows the voltage transfer characteristic of the amplifier circuit using type IT124 super-beta transistor, operating at \( V_{CE} = 1.0 \, V \), \( I_C = 0.075 \, mA \), \( R_L = 10.7 \, k\Omega \). The saturation emitter to collector voltage is 37.5 mV. The distance between the upper and lower output limiting levels is 1.76 volts. The slope of the linear region can be used to determine the voltage gain of the amplifier circuit, but the voltage divider at the input circuit has to be considered because the value shown on the graph is \( V_S \). Since the linear region is difficult to determine accurately from the graph, discussion of an alternate method is considered in the next section. But, if the operating point is set around the center of the transfer characteristic, we will have the linear region of the amplifier. The lower left portion of the transfer characteristic corresponds to the saturation region and the upper right portion corresponds to the cutoff region.

Fig. 4-5 is the voltage transfer characteristic of an amplifier circuit using a different super-beta transistor type PR1. This transistor is biased at the same point: \( V_{CE} = 1.0 \, V \), \( I_C = 0.075 \, mA \), \( R_L = 10.7 \, k\Omega \). The saturation collector to emitter voltage is 42.6 mV. The distance between upper and lower output limited levels is 1.84 volts. The linear region can be obtained around the center point of the transfer characteristic. The lower left portion of the transfer characteristic is saturation, while the upper right portion is cutoff.

Now let us examine these two transfer characteristics. For type PR1 super-beta transistor, the distance between upper and lower output
limited levels is larger by about 0.08 volt. This means type PR1 super-beta transistor has larger collector current. It also has a steeper slope and the bend at the saturation region is sharper. However, the two types are in general quite similar. The reason for these curves having hysteresis loops is that the phase angle between output and input signal voltages is slightly different. The operating frequency is 1 kHz.

When the value of the load resistance is changed, it will change the slope of the load line on the collector characteristic curve. If we again consider that the operating point is in the center of the active region, the circuit will amplify as before, except the output voltage amplitude will differ. Consider Figs. 4-6 and 4-7; they show the voltage transfer characteristics of the two super-beta transistor amplifiers with smaller values of load resistance. We see that the curves are very similar to the previous observations.

Fig. 4-6 shows the transfer characteristic of the amplifier circuit using type IT124 super-beta transistor, operating at $V_{CE} = 1.0\,V$, $I_C = 0.19\,mA$, $R_L = 3.4\,k\Omega$. The saturation collector-to-emitter voltage is 97.5 mV. The distance between the lower and upper output limited levels is 1.48 volts. The bend at the cutoff region is sharper than that at the saturation region. This is because at saturation, the collector current still keeps increasing somewhat.

Fig. 4-7 shows the transfer characteristic of type PR1 super-beta transistor, which is biased at $V_{CE} = 1.0\,V$, $I_C = 0.22\,mA$, $R_L = 3.4\,k\Omega$. The distance between the upper and lower output limited levels is 1.64 volts. The saturation collector-to-emitter voltage is 0.115 volt.
Fig. 4-4. Transfer characteristic of IT124 at $V_C = 1.0$ V,
$I_C = 0.075$ mA, $R_L = 10.7$ kΩ. Horizontal scale: $V_{\text{in}} - 2$ V/div.
Vertical scale: $V_o - 0.2$ V/div.

Fig. 4-5. Transfer characteristic of PR1 at $V_C = 1.0$ V,
$I_C = 0.075$ mA, $R_L = 10.7$ kΩ. Horizontal scale: $V_{\text{in}} - 2$ V/div.
Vertical scale: $V_o - 0.2$ V/div.

Fig. 4-6. Transfer characteristic of IT124 at $V_C = 1.0$ V,
$I_C = 0.19$ mA, $R_L = 3.4$ kΩ. Horizontal scale: $V_{\text{in}} - 2$ V/div.
Vertical scale: $V_o - 0.2$ V/div.

Fig. 4-7. Transfer characteristic of PR1 at $V_C = 1.0$ V,
$I_C = 0.22$ mA, $R_L = 3.4$ kΩ. Horizontal scale: $V_{\text{in}} - 2$ V/div.
Vertical scale: $V_o - 0.2$ V/div.
This curve has a sharper transition into saturation than into cutoff.

4-3 Determination of the Linear Region of the Amplifier Circuit

Distortionless amplification uses the linear region of the voltage transfer characteristic. Under small-signal conditions, the slope of the transfer characteristic determines the voltage gain of the amplifier. Since it is neither simple nor accurate to determine the linear region from the transfer characteristic, an alternate method is used. We plot the voltage gain as a function of the input signal amplitude. As long as the voltage gain remains constant, the amplifier is said to be in a linear region.

Fig. 4-8 shows the curves of voltage gain versus input signal voltage for both type PR1 and IT124 super-beta transistors, biased as given previously in Figs. 4-4 and 4-5. Fig. 4-9 is for a different load resistance, $R_L = 3.4 \, k\Omega$. We find that the linear regions of these two types of super-beta transistors are quite small and they are not ideal. For the type IT124 super-beta transistor, the linear region exists for input voltages below about 12 mV for both $R_L = 10.7 \, k\Omega$ and $3.4 \, k\Omega$. For type PR1 super-beta transistor, the linear region exists for signal voltages below about 12 mV when $R_L$ is $10.7 \, k\Omega$ and 16 mV when $R_L$ is $3.4 \, k\Omega$. When the input signal is less than 12 mV, we can be assured that this simple amplifier circuit is operated in the linear region, amplifying the waveform without noticeable distortion.

4-4 Comparison with Bipolar Transistor

Super-beta transistors are known to have high dc current gain, much larger than the bipolar transistor. After discussing the transfer
Fig. 4-8. Voltage gain of super-beta transistors as a function of input voltage.
$V_C = 1.0 \, V, \, R_L = 3.4 \, k\Omega, \, f = 1 \, kHz$

Fig. 4-9. Voltage gain of super-beta transistors as a function of input voltage.
characteristics of the super-beta transistors in the previous sections we now wish to see whether there is a large difference between these two devices under large signal conditions.

Two types of bipolar transistors are chosen for the comparison. The first one is the npn 2N956 transistor, the second one is the pnp 2N1381 transistor. Figs. 4-10 and 4-11 show the voltage transfer characteristics of these two transistor types. In order to compare with the super-beta transistor, we should use the same load resistance and set at the same operating point. Fig. 4-10 shows the transfer characteristic of the amplifier using type 2N956 transistor biased at $V_{CE} = 1.0 \text{ V}$, $I_C = 0.24 \text{ mA}$ and $R_L = 3.4 \text{ k}\Omega$. Fig. 4-11 is for type 2N1381 transistor, which is biased at the same point: $V_{CE} = -1.0 \text{ V}$, $I_C = 0.24 \text{ mA}$, and $R_L = 3.4 \text{ k}\Omega$. As we compare to Figs. 4-6 and 4-7, we find that in the linear region the curve is almost a straight line for the bipolar transistor; at the cutoff and saturation region, the bends sharply become horizontal, and it is easy to determine the boundaries of the linear region.

Figs. 4-12 and 4-13 show the transfer characteristics of the previous two transistors, but operating at different points. Fig. 4-12 is for type 2N1381 transistor, biased at $V_{CE} = -3.68 \text{ V}$, $I_C = 1.2 \text{ mA}$ and $R_L = 3.4 \text{ k}\Omega$. Fig. 4-13 is for type 2N956 transistor, biased at $V_{CE} = 7.9 \text{ V}$, $I_C = 2.15 \text{ mA}$ and $R_L = 3.4 \text{ k}\Omega$. We find that the curves have sharper transition from linear region to cutoff and saturation than that in Figs. 4-10 and 4-11.
Fig. 4-10. Transfer characteristic of 2N956 transistor at
\( V_C = 1.0 \text{ V}, I_C = 0.24 \text{ mA}, R_L = 3.4 \text{ k}\Omega \).
Horizontal scale: \( V_{\text{in}} - 2 \text{ V/div.} \)
Vertical scale: \( V_o - 0.2 \text{ V/div.} \).

Fig. 4-11. Transfer characteristic of 2N1381 transistor at
\( V_C = -1.0 \text{ V}, I_C = 0.24 \text{ mA}, R_L = 3.4 \text{ k}\Omega \).
Horizontal scale: \( V_{\text{in}} - 2 \text{ V/div.} \)
Vertical scale: \( V_o - 0.2 \text{ V/div.} \).

Fig. 4-12. Transfer characteristic of 2N1381 transistor at
\( V_C = -3.68 \text{ V}, I_C = 1.2 \text{ mA}, R_L = 3.4 \text{ k}\Omega \).
Horizontal scale: \( V_{\text{in}} - 10 \text{ V/div.} \)
Vertical scale: \( V_o - 1 \text{ V/div.} \).

Fig. 4-13. Transfer characteristic of 2N956 transistor at
\( V_C = 7.9 \text{ V}, I_C = 2.15 \text{ mA}, R_L = 3.4 \text{ k}\Omega \).
Horizontal scale: \( V_{\text{in}} - 10 \text{ V/div.} \)
Vertical scale: \( V_o - 2 \text{ V/div.} \).
CHAPTER V

NOISE OF THE TRANSISTOR

5-1 Definition

When designing an amplifier for very small signals, one can not neglect the noise produced by the transistor. Noise, in broad sense, can be defined as any unwanted disturbance that obscures or interferes with a signal. Noise in the transistor can be classified into three main types: thermal noise, shot noise, and $1/f$ noise.

Thermal noise is caused by the random thermally excited vibration of the electrons in a resistance. Whenever a resistance is at a temperature above absolute zero, the electrons are in random motion. This instantaneous current fluctuation produces a thermal noise voltage across the terminals. According to Nyquist's theorem, thermal noise can be expressed as

$$E_{\text{nth}} = \sqrt{4kTR\Delta f}$$

(5-1)

where:

- $k =$ Boltzmann's constant $= 1.38 \times 10^{-23}$ watt-sec/degree.
- $T =$ temperature of resistor in degrees Kelvin.
- $\Delta f =$ equivalent noise bandwidth of the measuring system in Hz.
- $R =$ resistance in ohms.

Since there is base resistance between the base contact and the active base region in the transistor, this resistance produces thermal noise.

In tubes, transistors and diodes there is shot noise. This is due to the fact that the total current in these devices is not smooth and continuous. It is the sum of pulses of current caused by the flow of
carriers each with one electronic charge. The value of the shot noise current is given by

$$I_{nsh} = \sqrt{2q I_{DC} \Delta f}$$

(5-2)

where:  
- $q = \text{electronic charge, } 1.6 \times 10^{-19} \text{ coulombs.}$
- $I_{DC} = \text{dc flowing in amperes.}$
- $\Delta f = \text{noise bandwidth in Hz.}$

There are two descriptions of shot noise in transistors as discussed by Van der Ziel.$^5$ One is that the current flowing in p-n junctions is due to the injection of minority carriers into the bulk region and their subsequent diffusion and recombination. The accurate way of describing the noise would be to introduce diffusion noise sources and generation-recombination noise sources for the minority carriers; another description represents the current as the passage of carriers across barriers, and since this constitutes a series of independent random events, one can expect full shot noise.

1/f noise has the spectral density of increasing without limit as frequency decreases. According to Fonger,$^5$ there are two types of 1/f noise, both with a low frequency spectrum: surface noise and leakage noise. Surface noise results from the fluctuating of minority carriers disappearing at the surface; this causes a fluctuating current to flow across the junction (or junctions) and it modulates the series resistance of the junction (or junctions). Leakage is caused by a thin conducting film bypassing the junction; it occurs at the perimeter of the junction and gives rise to a dc leakage current and a leakage conductance, which increase strongly with increasing bias. Spontaneous fluctuations in this leakage conductance can cause leakage noise.
In addition to thermal noise, shot noise, and 1/f noise, many silicon transistors, especially those of the planar-diffused type, show a type of low frequency noise known as burst or popcorn noise. This noise consists typically of random pulses of variable length. The source of burst noise is not clear at present, but it seems to be associated with shallow, heavily doped emitter junctions. It is believed that the appearance and disappearance of noise pulses is associated with a single trap in the space-charge region.

5-2 Equivalent Noise Model

In the previous section, transistor noise is discussed. These noise mechanisms can be shown in the hybrid-π model of Fig. 5-1. In this figure, the base resistance \( r_b \) is split into two parts \( r_{b1} \) and \( r_{b2} \); the 1/f noise source \( I_f \) and the shot noise \( I_b \) are in parallel with the resistance \( r_d \), and the burst noise \( I_{bb} \) is located much closer to the input terminals. \( E_b \) is the thermal noise of the base resistance \( r_b \), and \( I_c \) is the shot noise of the collector current.

The amount of thermal noise and shot noise can be determined theoretically, but 1/f noise and burst noise must be determined by measurement. For measurement simplicity, all the noise mechanisms may be referred to the input port. We define an equivalent input noise voltage \( E_{ni} \). Fig. 5-2 shows input port noise quantities. We can write

\[
E_{ni}^2 = E_n^2 + E_{nth}^2 + I_n^2 R_s^2 + 2CE_n I_n
\]

where \( E_n \) is the equivalent input noise voltage parameter of the transistor, \( I_n \) is the equivalent input noise current parameter of the transistor, \( R_s \) is the source resistance, and \( E_{nth} \) is the thermal noise of
the source resistance. Since noise parameters $E_n$ and $I_n$ may not be completely independent, a correlation coefficient $C$ is introduced in the equation. Because $C$ is zero over most of the frequency range, it usually can be neglected.

When all the noise mechanisms are referred to the input, the measuring system becomes noise free. We can draw an equivalent noise model as shown in Fig. 5-3. This is a universal noise model for any four terminal network, it can be applied to active as well as passive networks. The value of $E_{n_i}$ is determined as follows: with the signal source connected at terminals A and B in Fig. 5-3, measure the voltage at output terminals C and D. This value will give the system gain. Then disconnect the signal source and short circuit A-B, measure the output voltage. This is the equivalent output noise voltage of the system. Dividing the total equivalent output noise voltage by the system gain, we obtain the equivalent input noise voltage $E_{ni}$. The value of $E_{ni}$ is distinct for different source resistance values, as we can see from Eq. (5-3).

5-3 Noise Measurement Method

There are two general techniques for noise measurement. One is the sine wave generator method, and the other is the noise generator method. The second method needs a calibrated broad-band noise generator, while the first one uses general laboratory instruments, which are available at South Dakota State University, and is more applicable at low frequencies. Therefore, only the sine wave generator method is discussed in this section.
Fig. 5-1. Low frequency hybrid-pi noise model.

Fig. 5-2. Configuration of $E_{ni}$.

Fig. 5-3. Equivalent noise model.
The procedure for the sine wave generator method of noise measurement is:

1. Measure the total equivalent output noise voltage $E_{no}$ with a specific source resistance while the signal source terminal is short circuited.

2. Measure the output signal voltage $E_o$ with the same source resistance and determine the system voltage gain $K_t$ by dividing the output signal voltage $E_o$ by the signal source voltage $E_s$.

3. Calculate the equivalent input noise voltage $E_{ni}$ by dividing the output noise voltage $E_{no}$ with the system voltage gain $K_t$.

The circuit diagram of the noise measurement is shown in Fig. 5-4. Let us go through the circuit diagram stage by stage.

1. Signal generator: The input signal generator is a sine wave oscillator. GR type No.1210-C RC oscillator is used and disconnected before making noise measurements.

2. Attenuator: In order to avoid overdriving the super-beta transistor amplifier, an attenuator is needed. The attenuator serves two functions: it reduces the oscillator signal by a known factor and it provides a low impedance voltage source for measuring the amplifier gain. The values of $R_1$ and $R_2$ resistors are shown as 10.7 kΩ and 28.7Ω.

3. Voltmeter: This is a broadband ac voltmeter used to measure the signal voltage $E_s$. HP type 400E ac voltmeter which has a nominal bandwidth of 10 MHz is used. For noise measurement, the voltmeter is replaced by a shorting plug.

4. Source resistor $R_s$: To measure the noise of a transistor, a resistor $R_s$ equivalent to the source resistance is required. Low
Fig. 5-4. Noise measurement instrumentation.
Eq. (5-3) indicates that the total equivalent input noise voltage $E_{ni}$ depends upon the source resistance $R_S$. If the source resistance is made zero or very small, the terms $E_{n\text{th}}^2$ and $I_n^2R_S^2$ will be zero or very small. The total equivalent input noise voltage $E_{ni}$ is the equivalent input noise voltage parameter $E_n$. If the source resistance is made very large, the term $I_n^2R_S^2$ will dominate, because $E_{n\text{th}}^2$ is proportional to resistance while the $I_n^2R_S^2$ term is proportional to the square of resistance. Since $E_{ni}$ is mostly the $I_nR_S$ term, dividing by $R_S$ will give the equivalent input noise current parameter $I_n$. Therefore, to determine $E_n$, measure the total output noise with a small source resistance, while for $I_n$, measure the total output noise with a large source resistance. In this measurement, the values are chosen as 6.81Ω and 1 MΩ.

5. Transistor test circuit: The transistor under test is connected as an amplifier. The sine wave generator method applies equally well for measuring the noise of a single transistor, an integrated circuit, or a complete amplifier. When measuring noise over a wide range of collector currents and frequencies, biasing becomes a problem. The low-noise biasing method is discussed in the next section.

Careful packaging of the test circuit is important. As a rule of thumb, construct the test circuitry as compact as possible and place it in small shielded box. There is a positive correlation between the size of the box and pick-up noise. It is shown that 2" x 3" x 5" cast aluminum boxes do a very good job of shielding. In this measurement, attenuator, source resistance and test circuit are all connected on the
same circuit board, which can be put inside the shielded box. BNC connectors are used as the output terminals from the shielded box.

6. **Preamplifier**: Frequently, the output of the test stage will be as low as 20 nanovolts. Since wave analyzer and voltmeter require several microvolts, a low-noise decade amplifier with a gain of 10 or 100 after the test stage is needed. HP type 465A decade amplifier with gain of 20 dB or 40 dB and output noise less than 20 microvolts is used.

Ideally, the noise of the decade amplifier will not contribute to the noise of the transistor under test. However, when the test stage gain is low there may be additional noise. To test for added noise, replace the power supply connection of the test circuit with a shorting plug. The readings on the wave analyzer or voltmeter will be the output noise of the decade amplifier and wave analyzer or the filter and voltmeter. These values can be subtracted as the difference of the squares from the total output noise. The results will be the equivalent output noise of the test circuit. The added noise has to be measured at each test frequency.

7. **Wave analyzer**: For spectral or spot noise measurement, bandwidth limiting is required. The noise is measured in a specified noise bandwidth $\Delta f$. Two methods of noise measurement are illustrated in Fig. 5-4 as paths A and B. Path A uses a wave analyzer with bandwidth of several Hertz for narrow-band noise measurements, and path B uses a filter and voltmeter for broad-band noise measurements. Type GR 736A wave analyzer with noise bandwidth of 4 Hz is used.

We know that every frequency component of a noise waveform is randomly occurring with a random amplitude. It is shown in Reference [7]
that the measurement error $\sigma$ is inversely proportional to the square root of bandwidth and time constant:

$$\sigma = \frac{1}{\sqrt{2\gamma\Delta f}} \quad (5-4)$$

where: $\sigma$ = the error in measurement = rms fluctuation divided by the average value.

$\gamma$ = time constant.

$\Delta f$ = noise bandwidth.

This equation says that the longer the integration time and the wider the bandwidth, the less will be the error in measurement. For the same level of accuracy, a narrow-band measurement requires longer averaging time than a broad-band measurement does. Therefore, when the wave analyzer is used to measure the output noise, the output meter has large fluctuations which make it hard to read. In order for the meter to be readable, time-constant of the meter must be increased. The most common way to obtain a long time-constant is to parallel the meter with a capacitor. A low leakage tantalum electrolytic capacitor is preferable. It is found that when a 3300 $\mu$F capacitor parallels the meter, the needle fluctuates slowly and the value is readable. Since the meter readings are average values an ac voltmeter is used to calibrate the system when measuring the system gain. The correction factor of the meter is found to be 1.022 to change the average readings to rms values.

8. Filter: In broadband noise measurement, a bandpass filter determines the noise bandwidth of the system. The definition of noise bandwidth and how to determine it will be discussed in the following section. A KROHN-HITE solid-state variable filter is used as a band-
pass filter in the research discussed here.

9. AC voltmeter: A typical voltmeter is designed to measure constant amplitude, repeated waveforms. It is calibrated to indicate the rms amplitude of a sine wave, but does not usually respond to the rms value of the input waveform. When such a voltmeter measures noise, the waveform of which is neither sinusoidal nor constant amplitude, errors will arise. Therefore, to measure noise accurately requires three properties: the meter must respond to the noise power; it must have adequate bandwidth and crest factor. Crest factor is defined as the ratio of the peak value to the rms value of a signal. A true rms voltmeter is designed under these three conditions to indicate true rms value. HP type 3800 true rms voltmeter is used in this research.

5-4 Low-Noise Biasing

Biasing requires setting the proper dc voltages and currents in the circuit. These bias elements can add noise. Now let us discuss the method of biasing so that the biasing components do not add noise.

Fig. 5-5 shows the biasing of the super-beta transistor. The emitter bias resistor $R_E$ helps to set the desired emitter current. Also, it can maintain the dc emitter current despite changes in temperature and $\beta$. Since this is a test circuit, stability is not a very important problem. For emitter current between 0.05 mA to 0.2 mA, $R_E$ is 7320 ohms, while between 0.4 mA to 0.8 mA, $R_E$ is 4420 ohms. Base bias resistors $R_A$ and $R_B$ form a divider to hold the base voltage fixed. As the base current of the super-beta transistor is very small, $R_A$ and $R_B$ are chosen to be of equal value, 62.1 kΩ. The value of $R_I$ determines
the input resistance of the amplifier circuit, because that resistance is $R_I$ paralleled by the input resistance of the transistor itself. 2 MΩ is selected in order to maintain the high input resistance level. Capacitor $C_B$ is used to bypass the noise generated by $R_A$ and $R_B$. The reactance of $C_B$ must be small at the lowest frequency of interest in order to attenuate the noise. The value chosen is 220 μF. The capacitor $C_E$ is chosen as 200 μF to bypass the noise of $R_E$ and maintain sufficient gain. $R_E$ has two noise components: thermal noise of its resistance and excess current noise. In order to maintain the biasing of the transistor, capacitor $C_C$ is used to block the dc base current. Its value must be large enough so that it will not limit low frequency response. In other words, the reactance of the capacitor $X_C$ must be less than the sum of source resistance $R_S$ plus amplifier input resistance $R_{in}$ at the lowest frequency. An electrolytic capacitor can not be used, because its leakage current is comparable to the base current of the super-beta transistor. Therefore, a paper type capacitor of 0.22 μF is used in this research.

5-5 Noise Bandwidth Measurement

Noise bandwidth $\Delta f$ is not the same as 3 dB signal bandwidth. Noise bandwidth is the total integrated noise response while the signal bandwidth refers to the voltage gain roll-off frequency. In effect, there is one bandwidth for signal response and another for noise.

Noise bandwidth $\Delta f$ is the frequency width of an equal area rectangular shaped power transfer function of the system. In other words, noise bandwidth is equal to the area under the power gain curve divided
Fig. 5-5. Biasing of super-beta transistor.

Fig. 5-6. Illustration of noise bandwidth.

Where: $f_2 = 3$ dB point of the power curve.

$\Delta f = $ noise bandwidth in Hertz.
by the amplitude of the curve at the midband frequency \( f_0 \).

\[
\Delta f = \frac{1}{G'} \int_{-\infty}^{\infty} G(f) \, df \tag{5-5}
\]

where: \( \Delta f \) = noise bandwidth in Hz, \( G(f) \) = power gain at any frequency \( f \), \( G' \) = power gain at \( f_0 \). Since the power gain is proportional to the network voltage gain squared, noise bandwidth \( \Delta f \) is also:

\[
\Delta f = \frac{1}{2} \int_{-\infty}^{\infty} A_v^2(f) \, df \tag{5-6}
\]

where: \( A_v(f) \) = voltage gain as a function of frequency, \( A_{vo} \) = voltage gain at \( f_0 \).

In general, the mathematical voltage gain function \( A_v(f) \) is unknown; a graphical method is frequently used to determine the noise bandwidth. Fig. 5-6 shows the way of determining the noise bandwidth. It is the plot of the gain function of a typical broadband amplifier. To graphically determine the noise bandwidth, plot the power or voltage squared system gain versus frequency on a linear scale, and make a rectangle with the same maximum. The area of the rectangle is equal to the area under the power gain curve. Then, the bandwidth from zero to \( \Delta f \) is the noise bandwidth. In Fig. 5-6 we know that the sharper the amplifier's roll-off, the narrower the noise bandwidth.

5-6 Broad-band Noise Measurement

Noise can be measured at one frequency or over a frequency band as mentioned in Sec. 5-3, using wave analyzer or filter and ac voltmeter. Narrow-band noise or noise spectral density is used for analysis while broad-band noise indicates total system performance. In this section,
broad-band noise of the super-beta transistor is discussed first, and the narrow-band noise will be discussed in the next section. As shown in Fig. 5-4, when path B is selected, the system measures the broadband noise. This is the easier and more accurate noise measurement; it indicates the actual performance of a transistor, an amplifier or a system.

In broadband noise measurement, the bandwidth of the system is determined by the testing circuit or the filter, depending upon whether the bandwidth of the filter is greater or less than the bandwidth of the testing circuit. Two different filter bandwidths are used to measure the noise of the super-beta transistor. One is from 20 Hz to 100 kHz, another is from 20 Hz to 1 kHz. With 100 kHz bandwidth measurement, the filter bandwidth is larger than the bandwidth of the testing circuit. The noise bandwidths are determined graphically as noted in Sec. 5-5. Figs. 5-7 and 5-8 show the graphical determination of the noise bandwidths of the system using type IT124 and PR1 super-beta transistors at different source resistance values. We find from the graph that the noise bandwidths are dependent upon source resistance. Three different super-beta transistors of the same type have been measured. We call them No.1, No.2 and No.3. The results are shown in Figs. 5-9, 5-10, 5-11, and 5-12. With 1 kHz bandwidth, the filter bandwidth is smaller than that of the test circuit. Since the attenuation of the filter is 24 dB per octave beyond the cut-off frequency, the noise bandwidth approximately equals 1 kHz. This is also checked by the graphical method and found to be true.

A plot of equivalent input noise voltage versus source resistance
Fig. 5-7. Noise bandwidth of IT124, No. 1 at $V_C = 0.925 \text{ V}$, $I_C = 0.10 \text{ mA}$.

Fig. 5-8. Noise bandwidth of PR1, No. 1 at $V_C = 0.80 \text{ V}$, $I_C = 0.101 \text{ mA}$.
Fig. 5-9. Noise bandwidth of IT124, No. 2 at $V_C = 0.925$ V, $I_C = 0.101$ mA.

Fig. 5-10. Noise bandwidth of IT124, No. 3 at $V_C = 0.93$ V, $I_C = 0.10$ mA.
Fig. 5-11. Noise bandwidth of PR1, No.2 at $V_C = 0.70 \, V$, $I_C = 0.109 \, mA$.

Fig. 5-12. Noise bandwidth of PR1, No.3 at $V_C = 0.92 \, V$, $I_C = 0.10 \, mA$. 

The curves show the effect of noise on the performance of the system. These results indicate the importance of selecting the appropriate noise performance parameters for the optimal operation of the system.
with two different bandwidths, for three different super-beta transistors of type IT124, is shown in Fig. 5-13, and Fig. 5-14 for type PR1 super-beta transistors. The bias of these transistors is set close to $V_C = 1.0 \text{ V}$, $I_C = 0.10 \text{ mA}$.

Fig. 5-15 shows the equivalent input noise voltage versus emitter current at different source resistance of type IT124, No.1, super-beta transistor. These curves show that there is no optimum emitter current in order to bias the super-beta transistor for low noise performance.

5-7 Narrow-Band Noise Measurement

To specify the noise of a transistor for the design of an amplifier, the noise spectral density is a useful tool. Noise spectral density means the noise in one Hertz bandwidth. It is found by dividing the rms noise voltage by the square root of the bandwidth. A wave analyzer with a narrow bandwidth of several Hertz can be used to measure the noise centered at a particular frequency. Dividing this noise voltage by the square root of its bandwidth gives the noise spectral density. The noise spectral density illustrates the relative effects of low versus high frequency noise and helps to separate the contributions of the noise mechanisms. Two noise parameters $E_n$ and $I_n$ are measured for analysis of the noise of the super-beta transistors. As mentioned in Sec. 5-3, the values of $E_n$ and $I_n$ are determined at low and at high source resistance values.

Figs. 5-16 and 5-17 are the plots of equivalent input noise voltage spectral density versus frequency of type IT124 and PR1 super-beta transistors. Both types of super-beta transistors behave the same.
Fig. 5-13. Broadband noise of IT124 super-beta transistors for two noise bandwidths.
Fig. 5-14. Broadband noise of PR1 super-beta transistors for two noise bandwidths.
Fig. 5-15. Equivalent input noise voltage vs. collector current of IT124, No. 1 at $V_C = 1.0$ V.
Fig. 5-16. Input noise voltage parameter as a function of frequency of IT124 super-beta transistors.
Fig. 5-17. Equivalent input noise voltage as a function of frequency of the type PR1 super-beta transistors.
At high frequencies, these transistors have a flat noise spectral density. This represents the thermal noise and shot noise of the transistors. As we can see from Eqs. (5-1) and (5-2), these mechanisms have equal noise power in each Hertz of bandwidth. But at low frequency, the $E_n/\sqrt{\nu}$ value increases, at a rate that is inversely proportional to the frequency. This is the $1/f$ noise of the transistor. The frequency corner of type IT124 super-beta transistor is about 100 Hz, while that of type PR1 super-beta transistor is 200 Hz. As compared with the low noise bipolar transistor, we find that the super-beta transistor has larger equivalent input noise voltage spectral density and a sharper slope at low frequency.

The plots of equivalent input noise current spectral density versus frequency for type IT124 and PR1 super-beta transistors are shown separately in Figs. 5-18 and 5-19. We also find that when frequency decreases, the equivalent input noise current spectral density increases. This is due to the $1/f$ noise of the transistor. These super-beta transistors have smaller $I_n/\sqrt{\nu}$ values than the low noise bipolar transistor.

In Fig. 5-18, we find that the No.2 IT124 super-beta transistor has much larger $I_n^2/\text{Hz}$ values than the other two super-beta transistors. It is clear that there is additional noise in this unit. It might be burst noise, or it might be that the base-emitter junction of the super-beta transistor is avalanched, due to a turn-on or signal transient. When the base-emitter junction is avalanched, the noise may increase by 10 times. In order to find the difference, two pictures are taken from the scope using the KROHN-HITE filter. Fig. 5-20 is
Fig. 5-18. Equivalent input noise current as a function of frequency of
IT124 super-beta transistors.
Fig. 5-19. Equivalent input noise current as a function of frequency of PR1 super-beta transistors.
taken from No. 1 IT124 super-beta transistor, and Fig. 5-21 is taken from No. 2 IT124 super-beta transistor. Both transistors are operated at the same conditions, and we find that No. 2 IT124 super-beta transistor does have larger noise amplitude.
Fig. 5-20. Noise amplitude of IT124, No. 1 super-beta transistor at $V_C = 1.0 \, V$, $I_C = 0.10 \, mA$, $R_S = 1 \, M\Omega$. Filter bandwidth: 20 Hz to 100 kHz. Horizontal scale: 0.2 msec/div. Vertical scale: 0.10 V/div.

Fig. 5-21. Noise amplitude of IT124, No. 2 super-beta transistor at $V_C = 0.92 \, V$, $I_C = 0.103 \, mA$, $R_S = 1 \, M\Omega$. Filter bandwidth: 20 Hz to 100 kHz. Horizontal scale: 0.2 msec/div. Vertical scale: 0.10 V/div.
CHAPTER VI

CONCLUSIONS

As a result of this investigation, the following conclusions can be reached regarding super-beta transistors.

1. Not only does the super-beta transistor have very high current gain, it also has very high input resistance. In order to obtain the high current gain performance, it is recommended that the operating collector current be below 140 $\mu$A. This low current is preferable in the input stage of an operational amplifier.

2. A small signal h-parameter analysis of super-beta transistors is presented. It is found that this transistor has more than ten times the short-circuit current gain $h_{fe}$ and one hundred times the input resistance $h_{ie}$ of the common bipolar transistor. The other two parameters, $h_{oe}$ and $h_{re}$, are slightly larger. The values of parameters $h_{fe}$ and $h_{re}$ decrease as the collector current increases. This is opposite to the normal behavior of bipolar transistors.

3. When the super-beta transistor is connected as an amplifier, it exhibits normal voltage gain, very high current gain, high input resistance and output resistance in the range of kilo-ohm. The transistor has limited high frequency performance; it cannot be operated above several hundred kilo-Hertz.

4. Since the super-beta transistor has very high input resistance, the discussion of transconductance is quite interesting. It
was shown that the \( g_m \) value remains constant up to several mega-Hertz, and the phase angle changes from 180 degrees to 130 degrees in this frequency band.

5. Because the super-beta transistor operates at low voltage levels, it can not be used as a power amplifier. The linear region of the amplification of the transistor for the input base-to-emitter rms signal voltage limited to below 12 mV. Beyond this value, the transistor small-signal parameters no longer apply.

6. The super-beta transistor has larger equivalent input noise voltage parameter \( E_n \) and smaller equivalent input noise current parameter \( I_n \) than the low noise bipolar transistor. The 1/f noise of this transistor is quite prominent.

7. It is interesting to observe that there is some kind of burst noise in one of the super-beta transistors under test. This is apparent for a source resistance of 1 MΩ. This transistor shows higher values of equivalent input noise current spectral density.
REFERENCES


